CAE2200 / CAE2400

11.2GSPS / 5.6GSPS 12 位射频采样模数转换器（ADC）

1 特性

- 分辨率：12-bit，无失码
- 采样率：

  CAE2200: 11.2Gsps or 5.6Gsps(双通道模式)

  CAE2400: 5.6Gsps 或 2.8Gsps(双通道模式)
- 通道数：1 或 2
- 输入电压范围[Vpp,diff]：0.8V (typical)
- 模拟输入带宽：5.2 GHz
- 积分非线性 INL:

  CAE2200: ±6.0 LSB,

  CAE2400: ±4.7 LSB,

  微分非线性 DNL:

  CAE2200: +1.2/-0.7 LSB,

  CAE2400: +0.5/-0.5 LSB,
- 信噪比 SNR@1.09GHz:

  CAE2200：47.1 dB

  CAE2400：51.1 dB
- 无杂散动态范围 SFDR:

  CAE2200：63.8 dB

  CAE2400：64.0 dB
- 有效位 ENOB [Bit]:

  CAE2200：7.53 (typical)

  CAE2400：8.20 (typical)
- 16 通道 JESD204B 输出，最大通道速率 14.0Gbps，支持 8b/10b 编码，支持子类 1 确定性延迟
- 可选数字下变频器(DDC)： 可选滤波

  实数输出支持 1x,2x,3x,4x,6x, 8x,12x, 16x,24x,32x,48x,64x 抽取比例

  复数输出支持 2x,4x,6x,8x,16x,24x, 32x, 48x,64x,96x,128x 抽取比例

  每个 DDC 均具有四个独立的 48 位 NCO，支持快速调频。
- 模拟输入通道过压保护
- 片内温度二极管
- 低功耗：

  CAE2200：2.9W

  CAE2400：1.9W
- 工作温度：-40 to 105°C
- 封装：FCBGA196 (12mm x 12mm)

2 应用

- 示波器和宽带数字转换器
- 宽带通信系统
- 高速数据采集
- 通信测试仪（802.11ad，5G）
- 射频采样软件定义无线电 (SDR)
- 光谱测量

3 概述

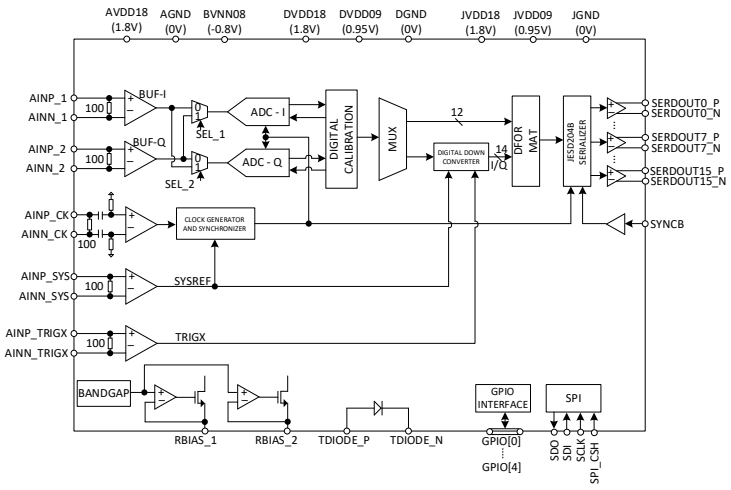
CAE2200 是一款 12 位，高速射频采样模数转换器 (ADC)，单通道模式下的最大采样率 11.2GSPS，双通道下的最大采样率为 5.6GSPS。

CAE2400 是一款 12 位，高速射频采样模数转换器 (ADC)，单通道模式下的最大采样率 5.6GSPS，双通道下的最大采样率为 2.8GSPS。

单通道或者双通道工作模式可在线编程配置，可用于开发灵活的硬件，以满足高通道数或宽瞬时信号带宽应用的需求。

CAE2200/CAE2400 采用高速 JESD204B 输出接口，工作温度支持-40 to 105°C，使用 FCBGA196 (12mm x 12mm) 封装。

4 功能框图



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5 修改历史

2025/3 Rev 1.3 寄存器说明增加 APB 读写寄存器, MAC Register, PMA PHY Register
2024/11 Rev 1.2
电气特性 SNR/SINAD/SFDR/ENOB 数据更新,
引脚 P10 的名称由 CONVST 改为 SPI_CSH,
勘误修正
2024/11 Rev 1.1 增加寄存器说明
2024/10 Rev 1.0
2024/05 Rev PreB

6 引脚配置和功能描述 (Pin Configuration and Functions)

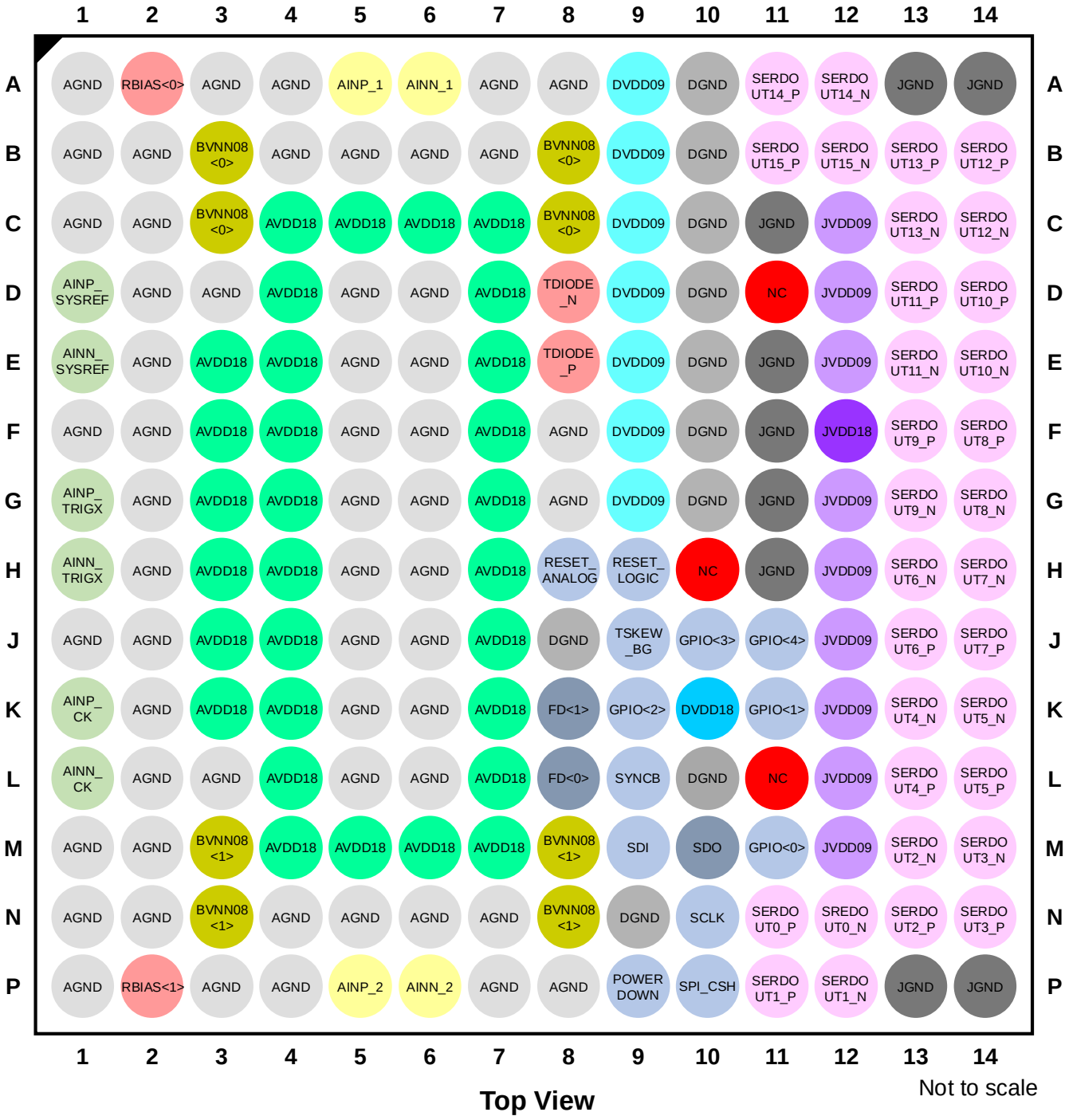


图 6-1. 196-Ball Flip Chip BGA

表 6-1. 引脚功能 (Pin Functions)

管脚序号	管脚名	类型	功能描述
A2, P2	RBIAS<0>, RBIAS<1>	输入	每个管脚接 12k 电阻，再接到地 注意 12k 电阻必须是高精度低温票电阻(建议采用 0.1%精度，温漂小于 25ppm/ºC)
A5	AINP_1	输入	双通道模式：模拟差分输入的正输入（I-channel） 单通道模式：模拟差分输入的正输入（I 或者 Q channel）。 它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。
A6	AINN_1	输入	双通道模式：模拟差分输入的负输入（I-channel） 单通道模式：模拟差分输入的负输入（I 或者 Q channel） 它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。
P5	AINP_2	输入	双通道模式：模拟差分输入的正输入（Q-channel） 单通道模式：不连接.单通道模式时候是通过 AINP_1/AINN_1 输入 它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。
P6	AINN_2	输入	双通道模式：模拟差分输入的负输入（Q-channel） 单通道模式：不连接。单通道模式时候是通过 AINP_1/AINN_1 输入 它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。
D1	AINP_SYSREF	输入	SYSREF 差分输入信号（正端），用于同步多 ADC 芯片数据时序给 FGPA. 它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求.
E1	AINN_SYSREF	输入	SYSREF 差分输入信号（负端），用于同步多 ADC 芯片数据时序给 FGPA. 它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求.
G1	AINP_TRIGX	输入	触发器(Trigger) X 差分信号(正端)，用于 DDC 模块的频率跳变。它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。
H1	AINN_TRIGX	输入	触发器(Trigger) X 差分信号(负端)，用于 DDC 模块的频率跳变。它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。
K1	AINP_CK	输入	主时钟差分信号(正端), 该管脚给芯片提供主时钟. 芯片内部通过 50 欧姆电阻 AC 耦合，但该管脚必须满足输入共模电压范围及摆幅的要求。
L1	AINN_CK	输入	主时钟差分信号(负端), 该管脚给芯片提供主时钟. 芯片内部通过 50 欧姆电阻 AC 耦合，但该管脚必须满足输入共模电压范围及摆幅的要求。

表 6-1. 引脚功能（续）

管脚序号	管脚名	类型	功能描述
E8	TDIODE_P	输入	温度二极管正（阳极）连接，通过外置温度传感器来监视芯片结温. 该管脚没被使用时，请悬空。
D8	TDIODE_N	输入	温度二极管正（负极）连接，通过外置温度传感器来监视芯片结温. 该管脚没被使用时，请悬空。
B3,B8,C3 , C8,M3,M8, N3,N8	BVNN08<0> BVNN08<1>	输入	它们连接到外部负 LDO 电源，该电源必须满足规范中的负电位和漏电流要求。
C4,C5,C6,C7 D4, D7 E3, E4, E7 F3, F4, F7 G3,G4,G7 H3,H4, H7 J3, J4, J7 K3, K4, K7 L4, L7 M4,M5,M6,M7	AVDD18	输入	1.8V 模拟 I/O 电源
A1,A3,A4 A7,A8 B1,B2,B4 B5,B6,B7 C1,C2,D2 D3,D5,D6 E2,E5,E6 F1,F2,F5 F6,F8,G2 G5,G6,G8 H2,H5,H6 J1,J2,J5 J6,K2,K5 K6,L2,L3 L5,L6,M1 M2,N1,N2 N4,N5,N6 N7,P1,P3 P4,P7,P8	AGND	输入	模拟地
A9,B9,C9, D9,E9,F9 G9	DVDD09	输入	0.95V 数字内核电源
K10	DVDD18	输入	1.8V 数字 I/O 电源
A10,B10 C10,D10 E10,F10 J8,G10,L10	DGND	输入	数字地
H8	RESET_ANALOG	输入	一旦提供了主时钟，该管脚对时钟产生器进行复位。高电平时复位，正常工作时保持低电平,1.8V 逻辑。
H9	RESET_LOGIC	输入	数字电路复位信号，高电平时复位，正常工作时保持低电平。 芯片上电时，芯片内部的 POR 复位了所有的数字电路，该复位信号可以忽略,1.8V 逻辑。
L8, K8	FD<0>, FD<1>	输出	快速检测管脚，FD<0> 对应 I-channel，FD<1> 对应 Q-channel，,1.8V 逻辑。
M11,K11 K9, J10 J11	GPIO<4:0>	输入	用于 DDC 的快速频率跳转。缺省配置时，这些管脚可以悬空,1.8V 逻辑。

表 6-1. 引脚功能（续）

管脚序号	管脚名	类型	功能描述
J9	TSKEW_BG	输入	该管脚可以发起后台时序偏差校准（background timing skew calibration），1.8V 逻辑。
L9	SYNCB	输入	JESD204B 同步信号。低电平时，JESD204B 与接收器正进行握手，握手完成时候，该管脚转为高电平,1.8V 逻辑。
P10	SPI_CSH	输入	SPI 片选使能信号, 0 将复位 SPI, 当 SPI 进行读写时，保持为 1, 1.8V 逻辑。
N10	SCLK	输入	主 SPI 时钟信号,1.8V 逻辑。
M9	SPI	输入	主 SPI 输入信号,1.8V 逻辑。
M10	SDO	输出	主 SPI 输出信号,1.8V 逻辑。
P9	POWERDOWN	输入	芯片断电管脚，输入高电平将芯片断电，正常工作时保持低电平, 1.8V 逻辑。
D11,H10,L11	NC	/	悬空，不连接
C12, D12 E12, G12 H12, J12 K12, L12 M12	JVDD09	输入	0.95V JESD204B 内核供电
F12	JVDD18	输入	1.8V JESD204B 接口 I/O 供电
A13, A14 C11, E11 F11, G11 H11, P13 P14	JGND	输入	JESD204B 接口地
N11 N12	SERDOUT0_P SERDOUT0_N	输出	Lane 0 差分 SerDes 输出对, 内接 100 欧姆电阻
P11 P12	SERDOUT1_P SERDOUT1_N	输出	Lane 1 差分 SerDes 输出对, 内接 100 欧姆电阻
N13 M13	SERDOUT2_P SERDOUT2_N	输出	Lane 2 差分 SerDes 输出对, 内接 100 欧姆电阻
N14 M14	SERDOUT3_P SERDOUT3_N	输出	Lane 3 差分 SerDes 输出对, 内接 100 欧姆电阻
L13 K13	SERDOUT4_P SERDOUT4_N	输出	Lane 4 差分 SerDes 输出对, 内接 100 欧姆电阻
L14 K14	SERDOUT5_P SERDOUT5_N	输出	Lane 5 差分 SerDes 输出对, 内接 100 欧姆电阻
J13 H13	SERDOUT6_P SERDOUT6_N	输出	Lane 6 差分 SerDes 输出对, 内接 100 欧姆电阻
J14 H14	SERDOUT7_P SERDOUT7_N	输出	Lane 7 差分 SerDes 输出对, 内接 100 欧姆电阻
F14 G14	SERDOUT8_P SERDOUT8_N	输出	Lane 8 差分 SerDes 输出对, 内接 100 欧姆电阻
F13 G13	SERDOUT9_P SERDOUT9_N	输出	Lane 9 差分 SerDes 输出对, 内接 100 欧姆电阻
D14 E14	SERDOUT10_P SERDOUT10_N	输出	Lane 10 差分 SerDes 输出对, 内接 100 欧姆电阻
D13 E13	SERDOUT11_P SERDOUT11_N	输出	Lane 11 差分 SerDes 输出对, 内接 100 欧姆电阻
B14 C14	SERDOUT12_P SERDOUT12_N	输出	Lane 12 差分 SerDes 输出对, 内接 100 欧姆电阻
B13 C13	SERDOUT13_P SERDOUT13_N	输出	Lane 13 差分 SerDes 输出对, 内接 100 欧姆电阻
A11 A12	SERDOUT14_P SERDOUT14_N	输出	Lane 14 差分 SerDes 输出对, 内接 100 欧姆电阻
B11 B12	SERDOUT15_P SERDOUT15_N	输出	Lane 15 差分 SerDes 输出对, 内接 100 欧姆电阻

7 技术规格 (Specifications)

7.1 电气特性 (Electrical Characteristics)

Parameter	Conditions	CAE2400			CAE2200			Unit
		Min	Typ	Max	Min	Typ	Max	
Analog Input								
Full-scale input range	Fully differential @ 1.09GHz		0.8			0.8		Vpp,diff
Input Termination	Single-channel, differential		50			50		Ω
	Dual-Channel, differential		100			100		Ω
Singled Input capacitance	Singled-ended to AGND		400			400		fF
Differential Input capacitance	Differential inputs		80			80		fF
Input Common Mode	$V_{CM,input}$	0.40	0.45	0.50	0.40	0.45	0.50	V
Input Signal Bandwidth	-3dB bandwidth		5.0			5.2		GHz
SerDes Output								
Differential Output Voltage	Normal mode	0.45		0.50	0.45		0.50	Vpp,diff
Output Common Mode Voltage	AC coupled	0.57	0.63	0.79	0.57	0.63	0.79	V
Output Termination	Differential		100			100		Ω
Clock Input								
Differential Input Voltage	100 ohm differential, on-chip	0.3	1	2	0.3	1	2	Vpp,diff
Input Common Mode Voltage	$V_{CM,CLKIN}$	0.2	0.3	0.4	0.2	0.3	0.4	V
Clock Frequency	F_{CLK}			2.8			5.6	GHz
Duty Cycle			50.0			50.0		%
Singled Input Capacitance	Singled-ended to AGND		400			400		fF
Differential Input Capacitance	Differential inputs		80			80		fF
SYSREF Input								
Differential Input Voltage	100 ohm differential, on-chip	0.5	1.0	2.0	0.5	1.0	2.0	Vpp,diff
Input Common Mode Voltage	$V_{CM,SYSREFIN}$		0.9			0.9		V
Frequency	Periodic mode		17.5	43.75		35	87.5	MHz
Pulse Width	Burst and Periodic modes	357.14			178.57			ps
Singled Input Capacitance	Singled-ended to AGND		450			450		fF
Differential Input Capacitance	Differential inputs		90			90		fF
Reference Voltage								
Internal Reference Voltage	Fully Differential	±0.375	±0.39	±0.405	±0.375	±0.39	±0.405	V
Tempco	From -40°C to 125°C		±50	±100		±50	±100	ppm/°C
DC Accuracy								
Resolution	DC code		12			12		bit
INL	Best-Fit	-6.0	±4.7	+6.0	-8.0	±6.0	+8.0	LSB
DNL	(no missing code)	-0.99	±0.5	+0.99	-0.99		+1.3	LSB
Offset Error	DC code error		±1			±1		mV
Code Error Rate	Whole chip		TBD			TBD		Error/ samples

7.1 电气特性 (Electrical Characteristics) （续）

Parameter	Conditions	CAE2400			CAE2200			Unit
		Min	Typ	Max	Min	Typ	Max	
AC Accuracy								
SNR	Fin = 170.4MHz, -1.0 dBFS		51.6			47.3		dBFS
	Fin = 170.4MHz, -2.0 dBFS		51.7			47.3		
	Fin = 170.4MHz, -6.0 dBFS		51.8			47.4		
	Fin = 1.09GHz, -1.0 dBFS		50.8			47.0		dBFS
	Fin = 1.09GHz, -2.0 dBFS		51.1			47.1		
	Fin = 1.09GHz, -6.0 dBFS		51.6			47.4		
	Fin = 2.41GHz, -1.0 dBFS		48.7			44.9		dBFS
	Fin = 2.41GHz, -3.0 dBFS		49.3			45.4		
	Fin = 2.41GHz, -6.0 dBFS		50.7			46.0		
	Fin = 3.95GHz, -1.0 dBFS		-			42.1		dBFS
	Fin = 3.95GHz, -3.0 dBFS		-			43.4		
	Fin = 3.95GHz, -6.0 dBFS		-			44.5		
	Fin = 4.85GHz, -1.0 dBFS		-			41.5		dBFS
	Fin = 4.85GHz, -3.0 dBFS		-			43.2		
	Fin = 4.85GHz, -6.0 dBFS		-			44.0		
SINAD	Fin = 170.4MHz, -1.0 dBFS		50.4			46.4		dBFS
	Fin = 170.4MHz, -2.0 dBFS		50.6			46.7		
	Fin = 170.4MHz, -6.0 dBFS		50.9			46.9		
	Fin = 1.09GHz, -1.0 dBFS		49.8			46.6		dBFS
	Fin = 1.09GHz, -2.0 dBFS		50.0			46.8		
	Fin = 1.09GHz, -6.0 dBFS		50.6			47.1		
	Fin = 2.41GHz, -1.0 dBFS		48.2			44.5		dBFS
	Fin = 2.41GHz, -3.0 dBFS		48.7			45.1		
	Fin = 2.41GHz, -6.0 dBFS		49.9			45.7		
	Fin = 3.95GHz, -1.0 dBFS		-			41.8		dBFS
	Fin = 3.95GHz, -3.0 dBFS		-			43.2		
	Fin = 3.95GHz, -6.0 dBFS		-			44.3		
	Fin = 4.85GHz, -1.0 dBFS		-			41.1		dBFS
	Fin = 4.85GHz, -3.0 dBFS		-			42.8		
	Fin = 4.85GHz, -6.0 dBFS		-			43.7		
SFDR	Fin = 170.4MHz, -1.0 dBFS		62.2			58.0		dBFS
	Fin = 170.4MHz, -2.0 dBFS		64.3			59.4		
	Fin = 170.4MHz, -6.0 dBFS		63.0			63.8		
	Fin = 1.09GHz, -1.0 dBFS		62.9			59.6		dBFS
	Fin = 1.09GHz, -2.0 dBFS		64.0			63.8		
	Fin = 1.09GHz, -6.0 dBFS		62.5			63.5		
	Fin = 2.41GHz, -1.0 dBFS		60.8			62.4		dBFS
	Fin = 2.41GHz, -3.0 dBFS		61.7			64.7		
	Fin = 2.41GHz, -6.0 dBFS		62.1			64.2		

7.1 电气特性 (Electrical Characteristics) （续）

Parameter	Conditions	CAE2400			CAE2200			Unit
		Min	Typ	Max	Min	Typ	Max	
SFDR	Fin = 3.95GHz, -1.0 dBFS		-			56.3		dBFS
	Fin = 3.95GHz, -3.0 dBFS		-			57.1		
	Fin = 3.95GHz, -6.0 dBFS		-			59.2		
	Fin = 4.85GHz, -1.0 dBFS		-			53.1		dBFS
	Fin = 4.85GHz, -3.0 dBFS		-			57.5		
	Fin = 4.85GHz, -6.0 dBFS		-			59.5		
ENOB	Fin = 170.4MHz, -1.0 dBFS		8.1			7.4		dBFS
	Fin = 170.4MHz, -2.0 dBFS		8.1			7.5		
	Fin = 170.4MHz, -6.0 dBFS		8.2			7.5		
	Fin = 1.09GHz, -1.0 dBFS		8.0			7.4		dBFS
	Fin = 1.09GHz, -2.0 dBFS		8.0			7.5		
	Fin = 1.09GHz, -6.0 dBFS		8.1			7.5		
	Fin = 2.41GHz, -1.0 dBFS		7.7			7.1		dBFS
	Fin = 2.41GHz, -3.0 dBFS		7.8			7.2		
	Fin = 2.41GHz, -6.0 dBFS		8.0			7.3		
	Fin = 3.95GHz, -1.0 dBFS		-			6.7		dBFS
	Fin = 3.95GHz, -3.0 dBFS		-			6.9		
	Fin = 3.95GHz, -6.0 dBFS		-			7.1		
	Fin = 4.85GHz, -1.0 dBFS		-			6.5		dBFS
	Fin = 4.85GHz, -3.0 dBFS		-			6.8		
	Fin = 4.85GHz, -6.0 dBFS		-			7.0		
Noise Floor Density	At 170.4MHz, -1 dBFS		-146.1			-144.8		dBFS/ √Hz
Speed								
ADC Sampling rate	Single-channel		5.6			11.2		GSPS
	Dual-Channel		2.8			5.6		GSPS
JESD204B lane rate	SerDes lane rate, 100 ohm termination	1.6875	7.0		1.6875	14.0		Gb/s
Power Supplies								
AVDD18,DVDD18,DRVDD2	1.8V power supplies	1.7	1.8	1.9	1.7	1.8	1.9	V
DVDD09,DRVDD,DVDD, VDD	0.95V power supplies	0.9	0.95	0.975	0.9	0.95	0.975	V
BVNN08	-0.8V negative power supplies	-0.85	-0.8	-0.75	-0.85	-0.8	-0.75	V
Current (1.8V supplies)	Normal mode, all bg calibrations enable & DDC off		761			1130		mA
Current (0.95V supplies)	Normal mode, all bg calibrations enable & DDC off		555			855		mA
Current (1.8V supplies)	Power down		53			53		mA
Current (0.95V supplies)	Power down		9			9		mA
Power Consumption	Normal mode, all bg calibrations enable & DDC off		1.9			2.9		W
Junction Temperature	T_{MIN} to T_{MAX}	-40		125	-40		125	°C
Long-Term Reliability	For Pro-longed use	-40		105	-40		105	°C

7.2 时间要求 (Timing Requirements)

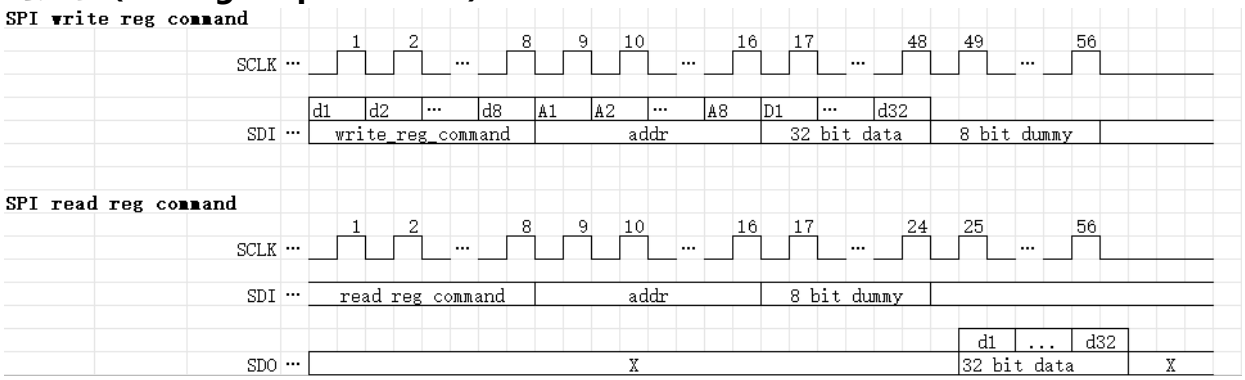
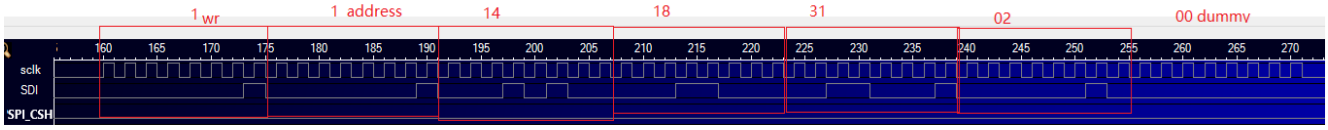


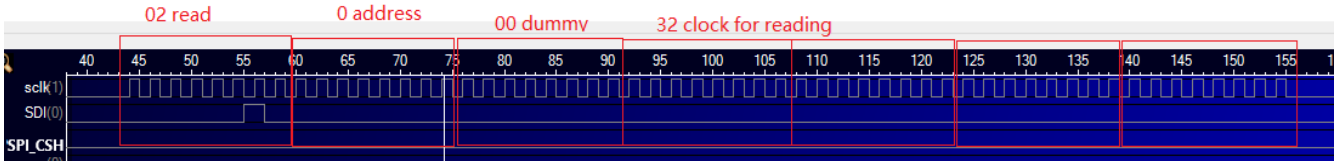
图 7-1. SPI 读写数据：接口波形

芯片复位后 SPI 读写寄存器，相关的信号 SPI_CSH 默认为 1。
SPI 读写寄存器需要 56bits。8 位命令字+ 8 位为地址+40 位数据。8 位命令字的控制为 8h01 写寄存器，8h02 读寄存器。
以 SPI 写第一寄存器 32'h14183102 为例：spi_wr_reg(8'h01,32'h14183102) 测试 pattern 波形：



前面八个 sclk， 对应 SDI 为 01，所以是 SPI 写。后面 8 个 SCLK，对应的是地址，数据为 01，表示写的是 01 寄存器。再接着的 32 个 SCLk， 对应的数据是 14,18,31,02 表示写入 01 寄存器的数值为 32'h14183102. 最后的 8 个 sclk， 对应的 SDI 为 0 ， 是无用的数据。（SPI_CSH=1）

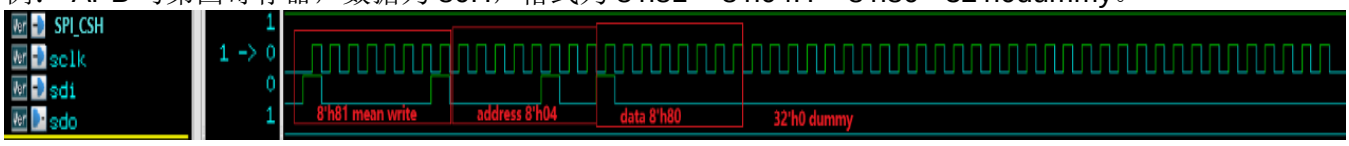
以 spi_rd_reg(8'h00,temp32b) 即读第 0 寄存器的结果为例，说明 SPI 读对应的波形：



前面八个 sclk， 对应 SDI 为 02，所以是 SPI 读命令。后面 8 个 SCLK，对应的是地址，数据为 00，表示读的是 00 寄存器。再接着的 8 个 sclk, 对应 SDI 数据为 0，为 8bits dummy， 最后面的 32 个 SCLk，对应的 SDI 数据是 0 ，而此时对应的 SDO 的输出为读出结果。（SPI_CSH =1）

测试激励信号是下降沿给 SDI 数据，芯片内部是上升沿抓数。芯片给出的 SDO 信号是 SCLK 上升沿给出，仪器下降沿去抓 SDO 结果。

对 JESD204B APB 寄存器的读写：
读写 APB 寄存器需要 56bits。8 位命令字+ 8 位地址+ 40 位数据。
8h81 写 APB 寄存器，8h82 读 APB 寄存器。
例： APB 写第四寄存器，数据为 80H，格式为 8'h81 + 8'h04H + 8'h80+ 32'h0dummy。



APB 读第四寄存器，8'h82 + 8'h04H + 8bits dummy+ 8bits data + 24bits dummy.
波形如下图所示：

7.3 典型特性 (Typical Characteristics)

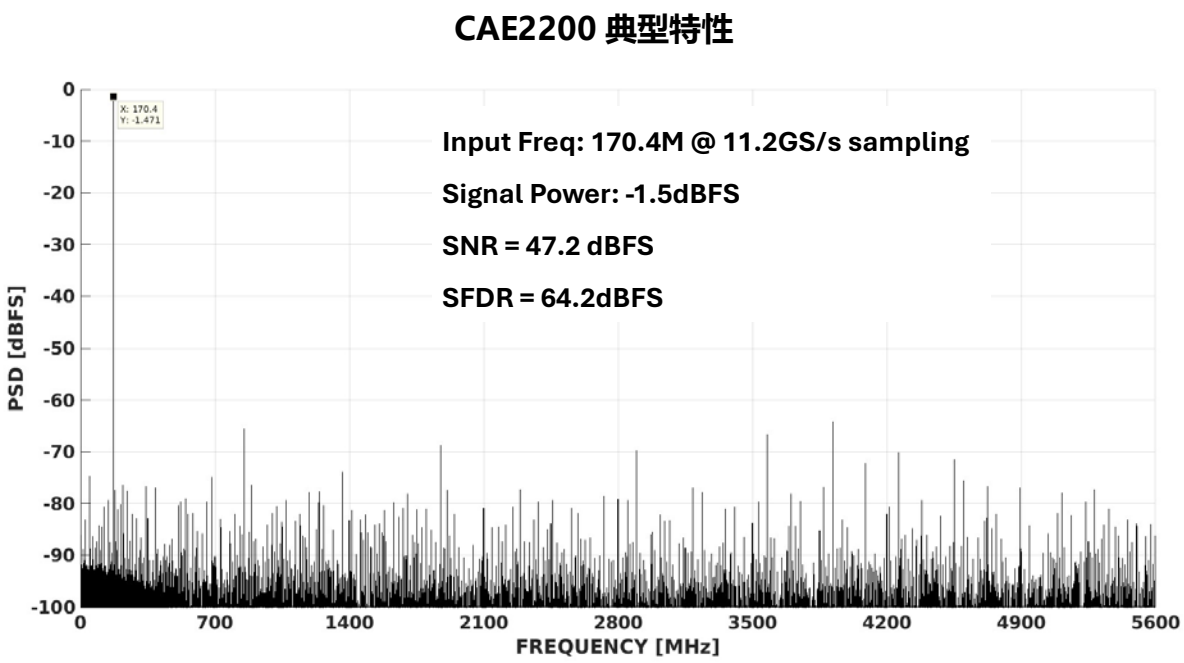


图 7-2. FFT at Fin = 170.4MHz, 11.2GS/s (CAE2200)

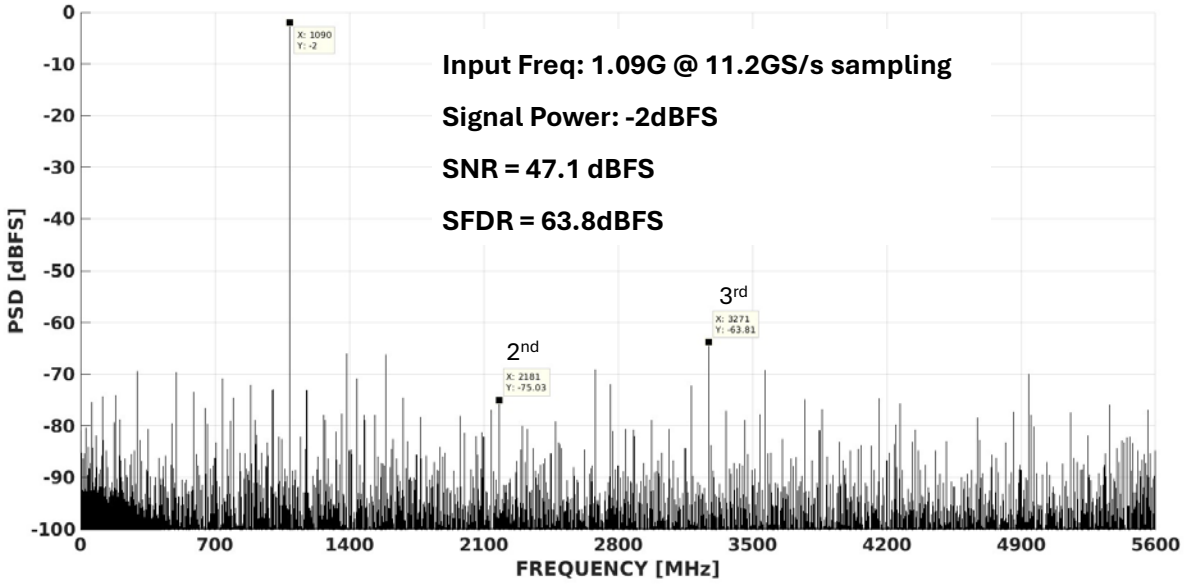


图 7-3. FFT at Fin = 1.09GHz, 11.2GS/s (CAE2200)

7.3 典型特性 (Typical Characteristics)

CAE2200 典型特性（续）

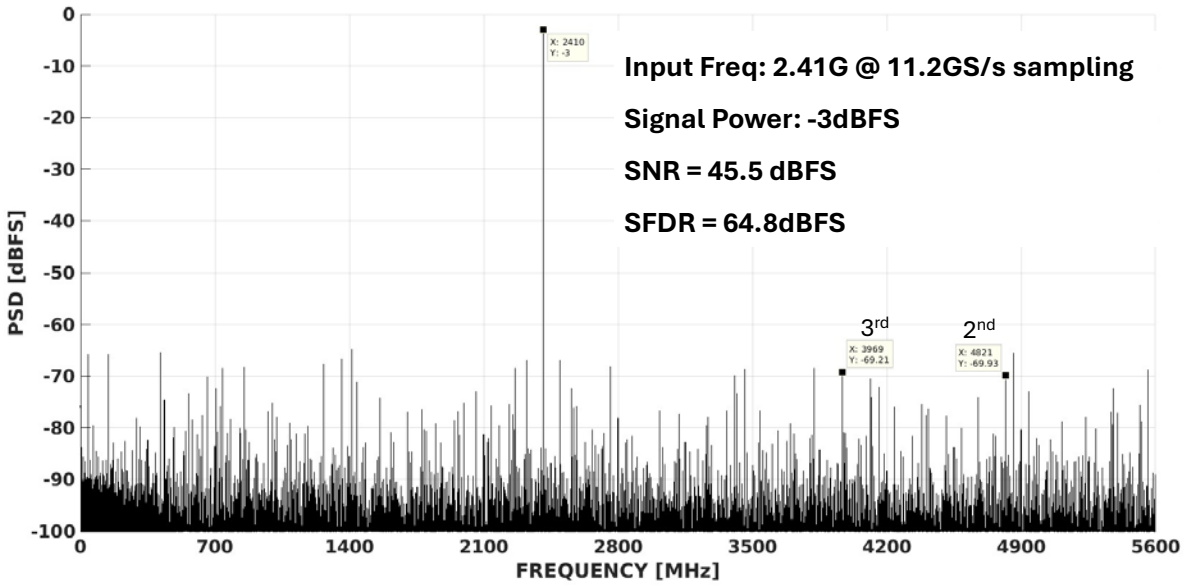


图 7-4. FFT at Fin = 2.41GHz, 11.2GS/s (CAE2200)

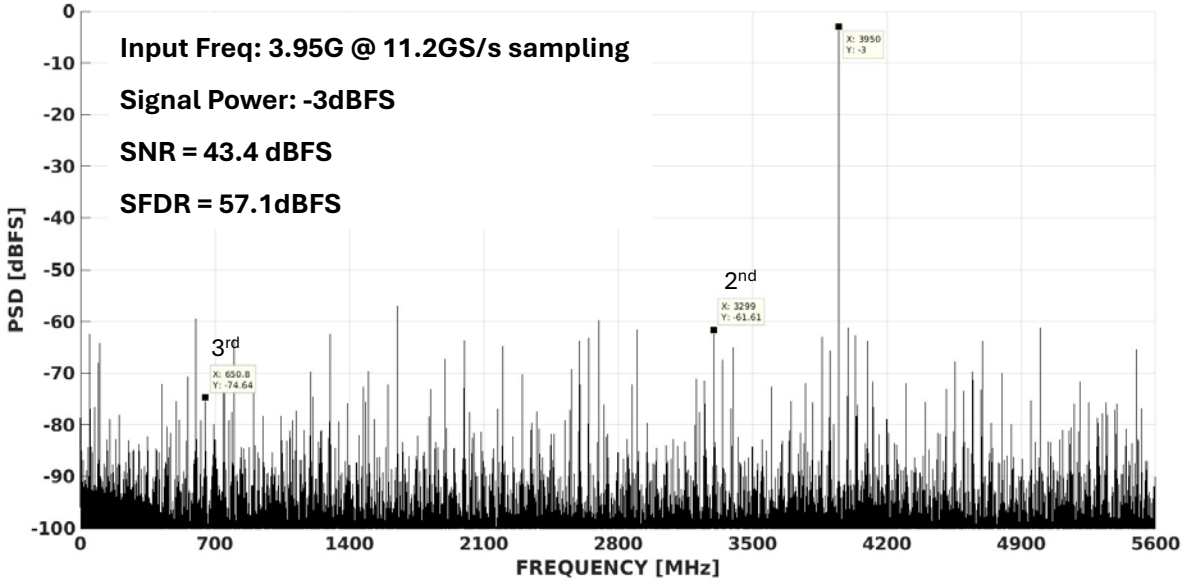


图 7-5. FFT at Fin = 3.95GHz, 11.2GS/s (CAE2200)

7.3 典型特性 (Typical Characteristics)

CAE2200 典型特性（续）

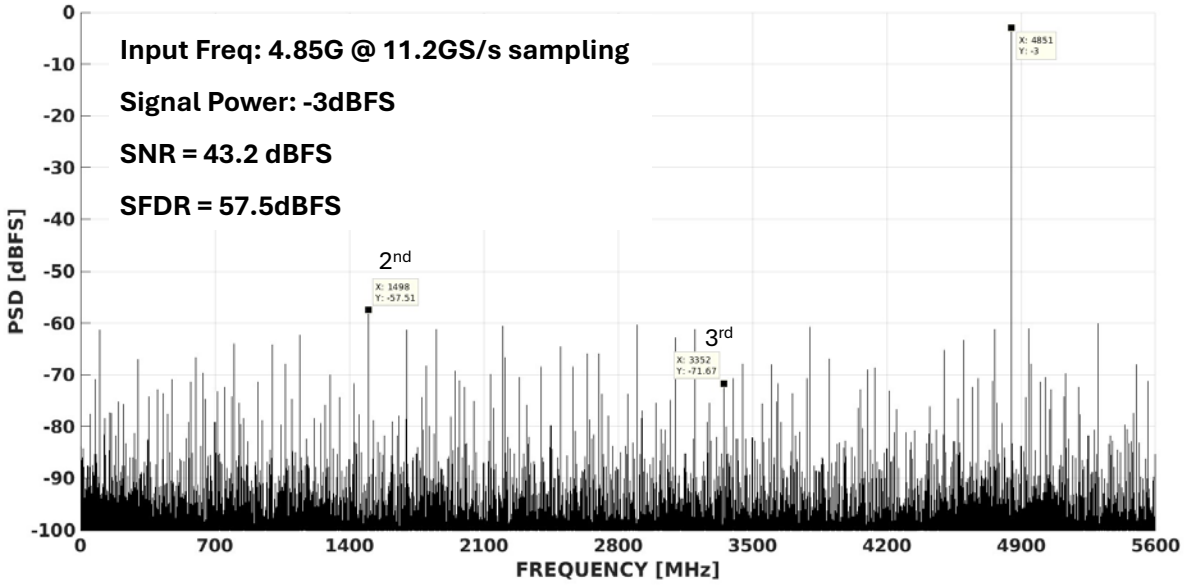


图 7-6. FFT at Fin = 4.85GHz, 11.2GS/s (CAE2200)

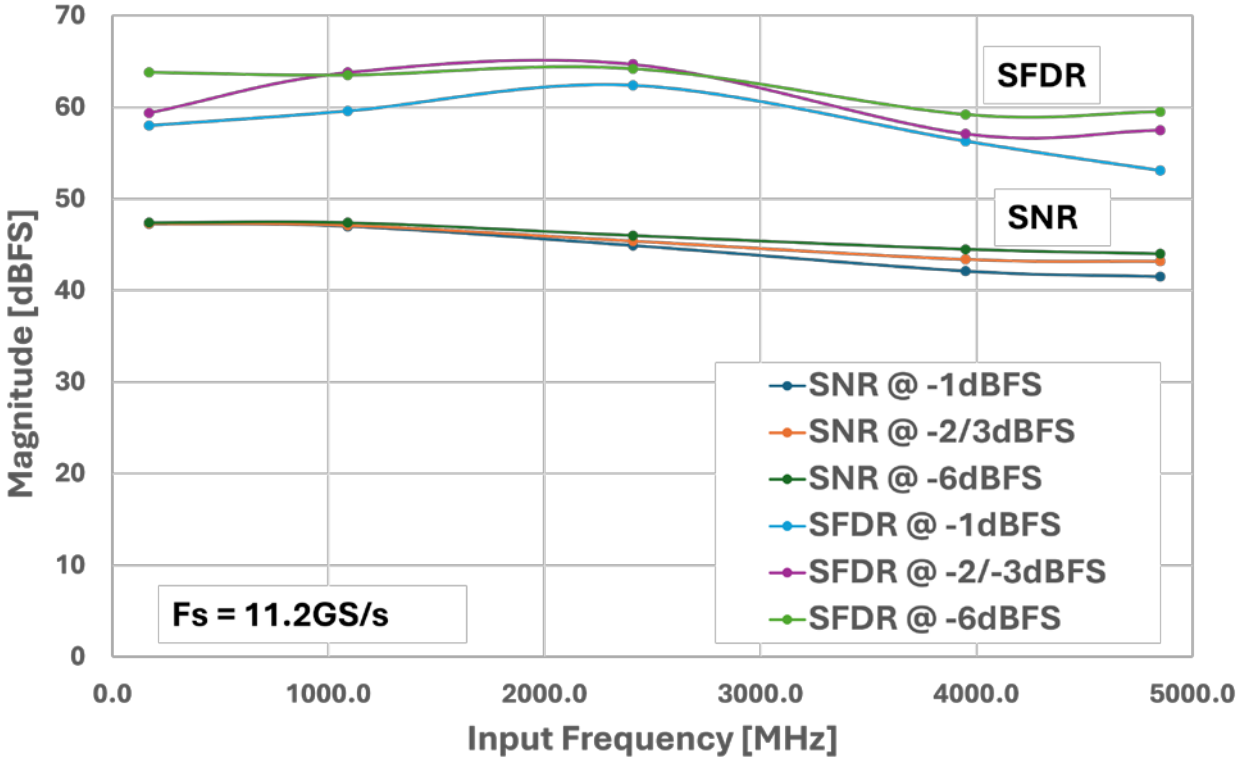


图 7-7. SNR/SFDR vs Input Frequency, 11.2GS/s (CAE2200)

7.3 典型特性 (Typical Characteristics)

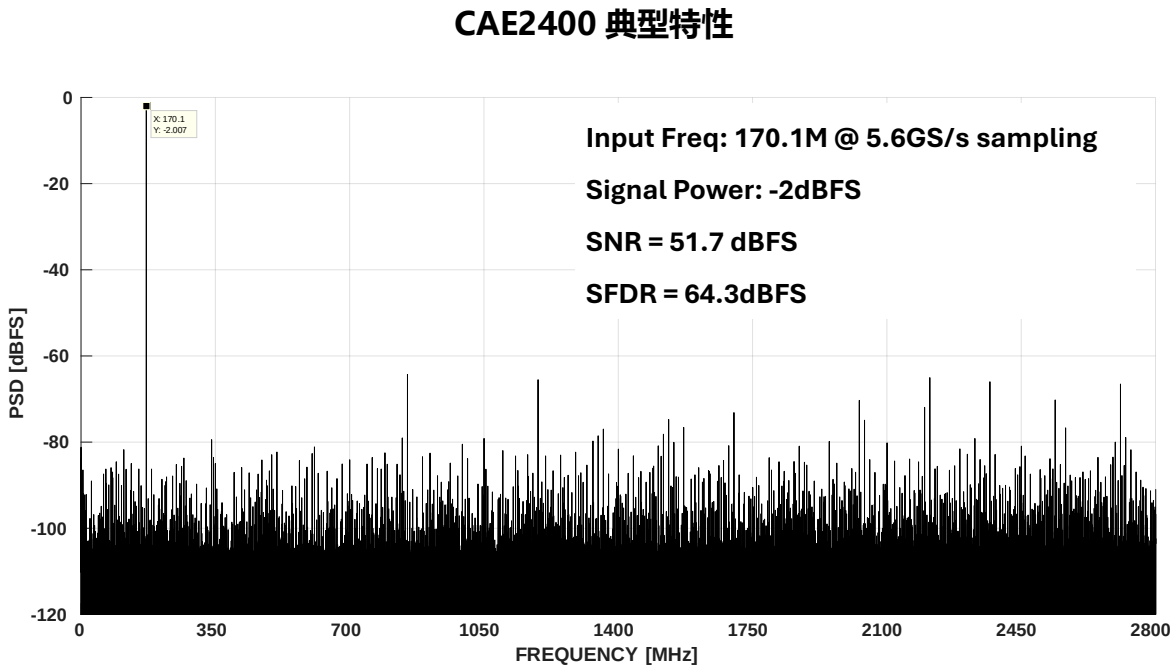


图 7.8. FFT at Fin = 170.1MHz, 5.6GS/s (CAE2400)

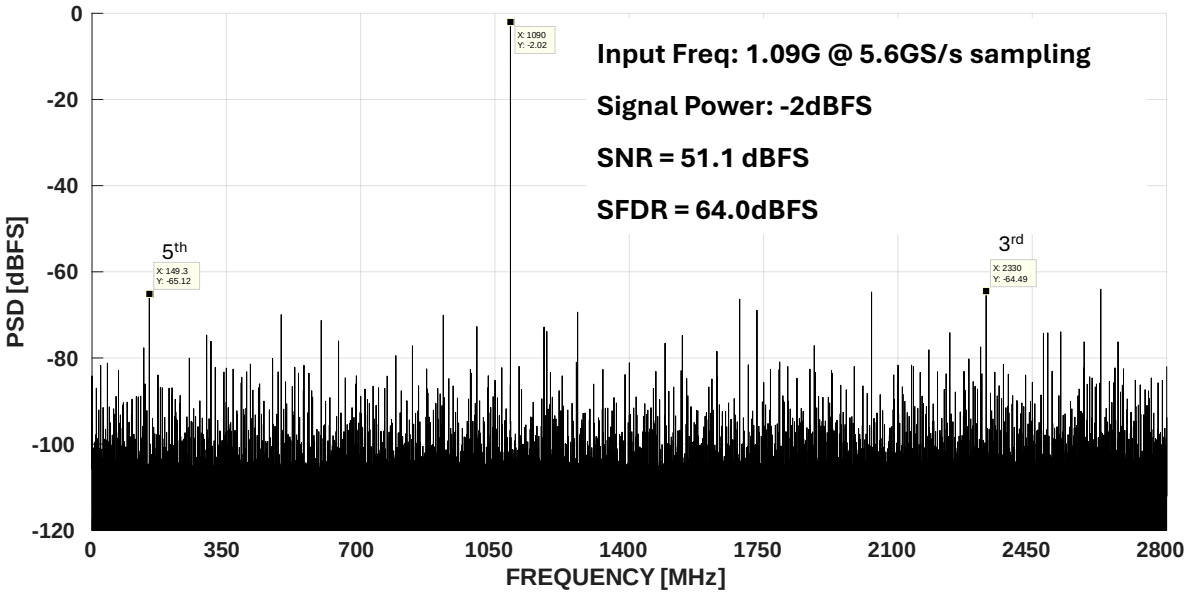


图 7-9. FFT at Fin = 1.09GHz, 5.6GS/s (CAE2400)

7.3 典型特性 (Typical Characteristics)

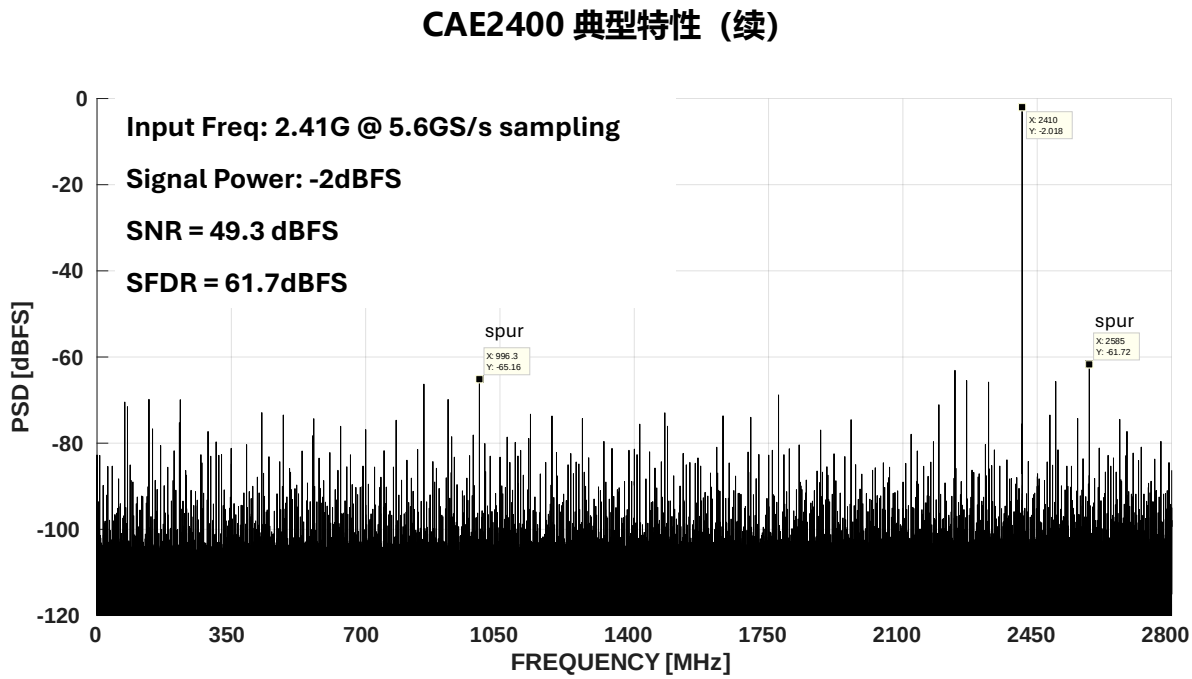


图 7-10. FFT at Fin = 2.41GHz, 5.6GS/s (CAE2400)

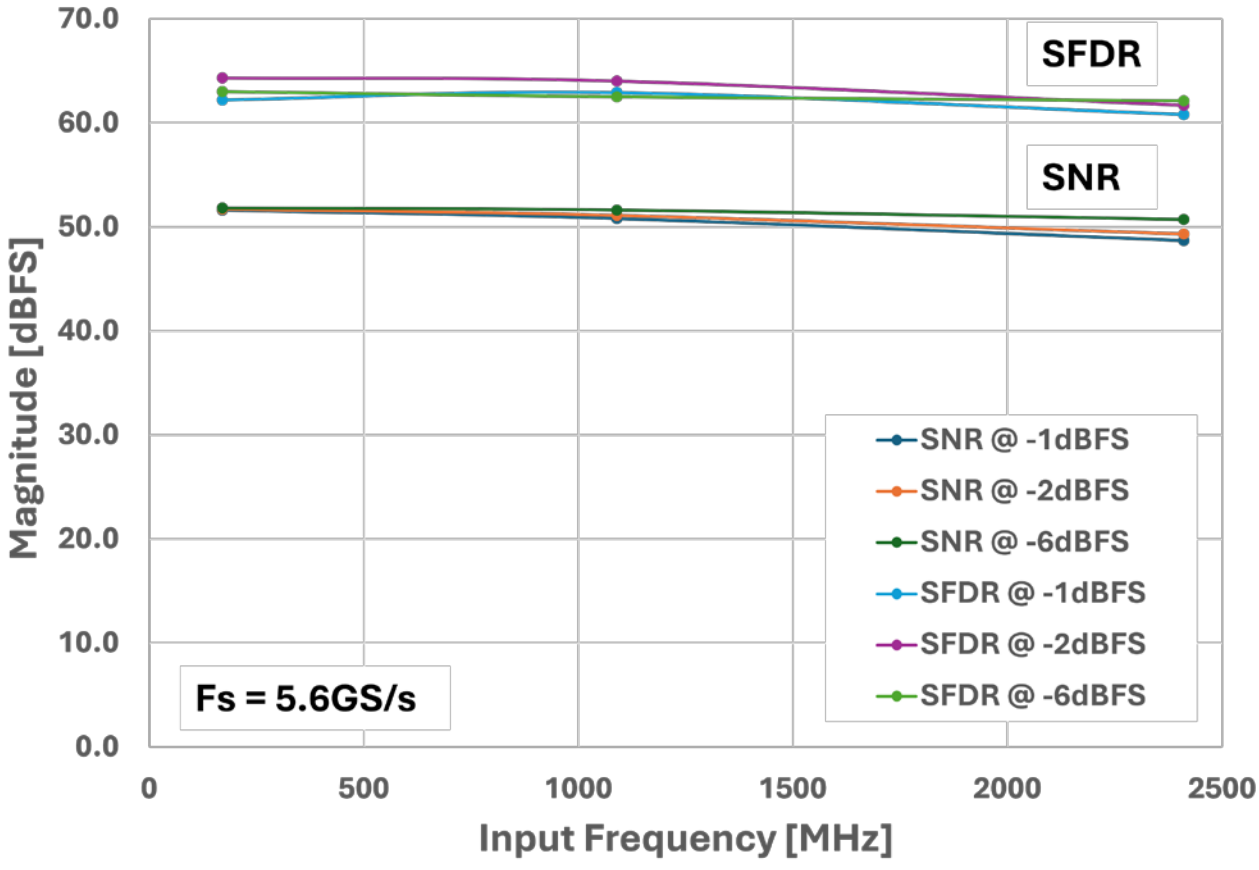


图 7-11. SNR/SFDR vs Input Frequency, 5.6GS/s (CAE2400)

8 详细说明 (Detailed Description)

8.1 概述 (Overview)

CAE2200 是一款 12 位，高速射频采样模数转换器 (ADC)，单通道模式下的最大采样率 11.2GSPS，双通道下的最大采样率为 5.6GSPS。

CAE2400 是一款 12 位，高速射频采样模数转换器 (ADC)，单通道模式下的最大采样率 5.6GSPS，双通道下的最大采样率为 2.8GSPS。

单通道或者双通道工作模式可在线编程配置，可用于开发灵活的硬件，以满足高通道数或宽瞬时信号带宽应用的需求。

CAE2200/CAE2400 采用高速 JESD204B 输出接口，工作温度支持-40 to 105°C，使用 FCBGA196 (12mm x 12mm) 封装。

8.2 功能框图 (Functional Block Diagram)

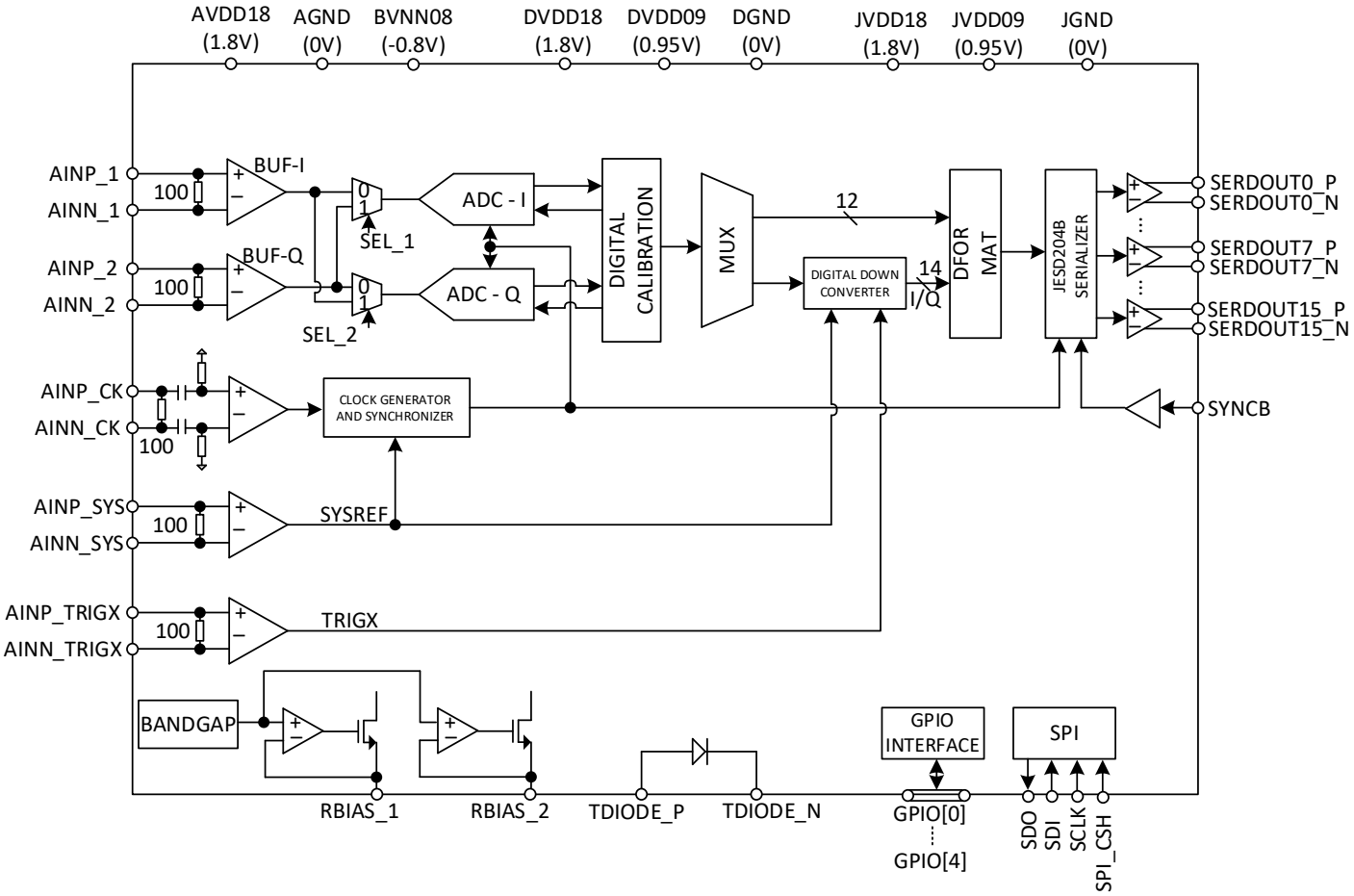


图 8-1. 功能框图

8.3 寄存器说明 (Memory Map)

控制寄存器（地址 8h05 32’ h0042_9448）

Bits	Name	Default	Descriptions
31	bg_always	1’b0	Background timing skew always do
30	bg_fpga	1’b0	When 1,reg03 FPGA rr write is update to tskew module;0 not update
29	tskew_hd_en	1’b0	Tskew_bg_pin is enable to control background timing skew
28:27	RVD		
26:24	bgpd_mode	3’h0	Background timing skew power down timing set(see below table)
22:20	tsrx_th	3’b100	000: 1;001 div2;010 div4;011div8,100div16 : timing skew matrix reuslt/N for rr
19	tsfir_en	1’b0	1:Timing skew input FIR enable;default 0 : disable
18	Dual_mode	1’b0	default0: 16ch; 1 dual 8ch
17	fg_mode_spi	1’b1	force finecap msb result=1
16	sel_otp_data	1’b0	Timing skew mode1/2 start from otp value (avoid many time to get better result)
15:14	bg_thres	2’b10	background timing skew threshold
13:12	bg_mode	2’b01	background timing skew mode
11	mid_tskew	1’b0	Background timing skew mode0 start from middle value1000_0000
10:8	tskew_mode	3’b001	Timing skew discard/average samples setting
7	inv_ts_mode	1’b0	Timing skew sgn result inverse
6:4	bg_ts_mode	3’b100	Background timing skew loop number
3:2	bg_repeat	2’b10	M_threshold for +/- as one big loop
1	tskew_bg	1’b0	Background timing skew enable
0	tskew_fg	1’b0	Foreground timing skew enable

控制寄存器（地址 8h06 32’ h4000_0ac7）

Bits	Name	Default	Descriptions
31:8	RVD		
7	p2SnOf	1’b1	code16 output 2's code(default) or offset code
6:0	RVD		

DDC 控制寄存器 (地址 8h07　32’ h0010_0000)

Bits	Name	Default	Descriptions
31:0	PST	32’h0010_0000	profile timer number

DDC 控制寄存器 (地址 8h08　32’ h0301_0000)

Bits	Name	Default	Descriptions
31:27	RVD		
26:24	{sync_en,sync_next, trig_rst_en}	3’b011	Register setting description SYSREF_x edge used to synchronize the PAWs 100 all subsequent edges for SYSREF_x signal reset all the PAWs in the chip 110 the next valid edge of SYSREF_x signal reset all the PAWs in the chip 001 all edges of SYSREF_x signal after TRIGGER signal reset all the PAWs in the chip 011 the next valid edge of SYSREF_x signal after TRIGGER signal reset all the PAWs in the chip
23:20	nco_nu_mode	4’h0	Nco number mode.0:NCO from reg;1 NCO from edge;2: NCO from GPIO; 3: NCO from profile select timer
19:18	reg_nu	2’b00	Nco number from register : choose one of 4NCO
17	RVD		
16	PD_TRIG	1’b1	1 power down trig ana,0 power on : default 1
15:8	Sysref_delay	8’h00	Sysref input delay
7:0	Trig_delay	8’h00	Trig input delay

DDC 控制寄存器 (地址 8h09　32’ h8001_4000)

Bits	Name	Default	Descriptions
31	ddc_soft_rstb	1’b1	Write 0 will reset ddc module
30:17	RVD		
16	RVD	1’b1	should write to 1'b0 if DDC
15:13	ddc_mac_mode	3’b100	DDC MA average number.0: 2^14, 1 2^15; 2 2^16 ... 6 2^20 ; 7 2^21
12	ddc_debug_mode	1’b0	1:DDC result MA from SPI; 0 from MA module
11	ddc_test_mode	1’b0	The input sampls are forces to positive full scale and the NCO is enabled. This test mode allows the NCOs to directly drive the decimation filters
10	ddc_gain_6db	1’b0	DDC gain 6DB
9	ddc_c2r_en	1’b0	DDC Complex to real enable
8	hb1_en	1’b0	DDC Hb1 FIR enable

Bits	Name	Default	Descriptions
7	tb2_en	1'b0	DDC Tb2 FIR enable
6	hb2_en	1'b0	DDC Hb2 FIR enable
5	hb3_en	1'b0	DDC Hb3 FIR enable
4	hb4_en	1'b0	DDC Hb4 FIR enable
3	hb5_en	1'b0	DDC Hb5 FIR enable
2	hb6_en	1'b0	DDC Hb6 FIR enable
1	hb7_en	1'b0	DDC Hb7 FIR enable
0	ddcen	1'b0	DDC enable

DDC 控制寄存器 for PHASE: only 4 NCO support if 16ch mode, set phas0—phase3.
in dual_mode, phase4--phase7 for adc2

Bits	Name	Default	Descriptions
47:0	{reg68[15:0] ,reg60[31:0]}	48'd32056872347602	Phase0: 41 degree (41/360) * 2^48
47:0	{reg68[31:16],reg61[31:0]}	48'd32056872347602	Phase1: 41 degree (41/360) * 2^48
47:0	{reg69[15:0] ,reg62[31:0]}	48'd32056872347602	Phase2:41 degree (41/360) * 2^48
47:0	{reg69[31:16],reg63[31:0]}	48'd32056872347602	Phase3:41 degree (41/360) * 2^48
47:0	{reg6a[15:0] ,reg64[31:0]}	48'd30493122476988	Phase4:39 degree (39/360) * 2^48
47:0	{reg6a[31:16],reg65[31:0]}	48'd30493122476988	Phase5:39 degree (39/360) * 2^48
47:0	{reg6b[15:0] ,reg66[31:0]}	48'd30493122476988	Phase6:39 degree (39/360) * 2^48
47:0	{reg6b[31:16],reg67[31:0]}	48'd30493122476988	Phase7:39 degree (39/360) * 2^48

DDC 控制寄存器 for FTW only 4 NCO support if 16ch mode, set FTW0--FTW3.
in dual_mode, FTW4--FTW7 for adc2

Bits	Name	Default	Descriptions
47:0	{reg50[15:0] ,reg6C[31:0]}	48'd136339441844233	FTW0:
47:0	{reg50[31:16],reg6D[31:0]}	48'd32985348833280	FTW1:
47:0	{reg51[15:0] ,reg6E[31:0]}	48'd65970697666560	FTW2:
47:0	{reg51[31:16],reg6F[31:0]}	48'd136339441844233	FTW3:
47:0	{reg56[15:0] ,reg52[31:0]}	48'd136339441844233	FTW4:
47:0	{reg56[31:16],reg53[31:0]}	48'd32985348833280	FTW5:
47:0	{reg57[15:0] ,reg54[31:0]}	48'd67114189759447	FTW6:
47:0	{reg57[31:16],reg55[31:0]}	48'd136339441844233	FTW7:

APB 读写寄存器

Begin Address	End Address	Range	module
0x00	0x7F	7bits	JESD204B MAC
0x80	0xFF	7bits	JESD204B PMA PHY

MAC Register

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x000	version_1	[7:0]	version_1		version number 1	0x20	R
0x001	version_2	[7:0]	version_2		version number 2	0x23	R
0x002	version_3	[7:0]	version_3		version number 3	0x05	R
0x003	version_4	[7:0]	version_4		version number 4	0x31	R
0x004	test	[7:0]	test_reg		reg for r/w test.	0x0	R/W
0x005	global_ctrl	[7]	PMA_pwrdn	0 1	204B IP power down control bit normal work power down	0x0	R/W
		[6:0]	Reserved		Reserved.	0x0	R
0x010	Sync mode	[7:3]	Reserved		Reserved.	0x0	R
		[2:1]	SYSREF± mode select	0 1 10	Disabled. Continuous. One-shot.	0x0	R/W
		[0]	Synchronization mode	0	JESD204B synchronization mode. The SYSREF signal resets all internal clock dividers. Use this mode when synchronizing multiple chips as specified in the JESD204B standard. If the phase of any of the dividers must change, the JESD204B link goes down.	0x0	R/W
				1	Timestamp mode. The SYSREF signal does not reset internal clock dividers. In this mode, the JESD204B link and the signal monitor are not affected by the SYSREF signal. The SYSREF signal timestamps a sample as it passes through the ADC and is used as a control bit in the JESD204B output word.		
0x011	sync error report	[7]	sync error cnt clear	0	1: clear error cnt	0x0	R/W
		[6:0]	sync error cnt	0	error cnt	0x0	R
0x012	User Pattern 1 LSB	[7:0]	User Pattern 1 [7:0]		User Test Pattern 1 least significant byte.	0x0	R/W
0x013	User Pattern 1 MSB	[7:0]	User Pattern 1 [15:8]		User Test Pattern 1 least significant byte.	0x0	R/W
0x014	User Pattern 2 LSB	[7:0]	User Pattern 2 [7:0]		User Test Pattern 2 least significant byte.	0x0	R/W
0x015	User Pattern 2 MSB	[7:0]	User Pattern 2 [15:8]		User Test Pattern 2 least significant byte.	0x0	R/W
0x016	User Pattern 3 LSB	[7:0]	User Pattern 3 [7:0]		User Test Pattern 3 least significant bits.	0x0	R/W
0x017	User Pattern 3 MSB	[7:0]	User Pattern 3 [15:8]		User Test Pattern 3 least significant bits.	0x0	R/W
0x018	User Pattern 4 LSB	[7:0]	User Pattern 4 [7:0]		User Test Pattern 4 least significant bits.	0x0	R/W
0x019	User Pattern 4 MSB	[7:0]	User Pattern 4 [15:8]		User Test Pattern 4 least significant bits.	0x0	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x01A	Output Mode Control	[7:6]	Reserved		Reserved.	0x0	R/W
		[5:4]	Converter control Bit 2 selection	0 1 10 11	Tie low (1'b0). control bit0 SYSREF Tie high(1'b1).	0x0	R/W
		[3:2]	Converter control Bit 1 selection	0 1 10 11	Tie low (1'b0). control bit0 SYSREF Tie high(1'b1).	0x0	R/W
		[1:0]	Converter control Bit 0 selection	0 1 10 11	Tie low (1'b0). control bit0 SYSREF Tie high(1'b1).	0x0	R/W
0x01B	PLL control	[7:4]	JESD204B lane rate control	0000 0001 0010 0011 0100 0101 0110	13.5~17G 8.5~13.5G 6.75~8.5G 4.25~6.75G 3.375~4.25G 2.125~3.375G 1.6875~2.125G	0x0	R/W
		[3:0]	ADC_num	0000 0001 0010	1 adc 2 adc 4 adc	0x0	R/W
0x01C	PLL status	[7]	clear_loss_lock	0 1	no action clear bit[1]	0x0	R/W
		[6:2]	Reserved	0	Reserved.	0x0	R
		[1]	PLL loss of lock	1	Loss of lock sticky bit. Indicate a loss of lock has occurred at some time. Cleared by setting bit[7].	0x0	R
		[0]	PLL lock status	0 1	Not locked. Locked.	0x0	R
0x01D	JESD204B Link status	[7:3]	Reserved		Reserved.	0x0	R
		[2]	sysref_sync_done		received sysref signal	0x0	R
		[1]	link_ready		pma fsm reset done	0x0	R
		[0]	tx_ready		clk_char&clk_samp reset done.	0x0	R
0x01E	pdiv/debug_ctrl	[5]	Reserved	0	Reserved.		
		[5]	Reserved	0	Reserved.		
		[4]	Reserved	0	Reserved.		
		[3:0]	debug_sel		debug pin select control	0x0	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x01F	DCM	[7]	Reserved	0	Reserved.		
		[6:0]	DCM	0000000 0000001 0000010 ..... 1111110 1111111	Decimation ratio = 1. Decimation ratio = 2. Decimation ratio = 3. ..... Decimation ratio = 127. Decimation ratio = 128.		
0x020	JESD204B Link Control 1	[7]	Standby mode	0 1	Standby mode forces zeros for all converter samples. Standby mode forces code group synchronization (K28.5 characters).	0x0	R/W
		[6]	Tail bit(t) PN	0 1	Disable. Enable.	0x0	R/W
		[5]	Syncb_error_disable	0 1	Subclass 1 or Subclass 2 receiver devices shall indicate the detection of such an error by activating the SYNC~ signal for exactly 2 frame periods. Disable.	0x0	R/W
		[4]	Lane synchronization	0 1	Disable FACI uses /K28.7/. Enable FACI uses /K28.3/ and /K28.7/.	0x1	R/W
		[3:2]	ILAS sequence mode	00 01 11	Initial lane alignment sequence disabled (JESD204B Section 5.3.3.5). Initial lane alignment sequence enabled (JESD204B Section 5.3.3.5). Initial lane alignment sequence always on test mode. JESD204B data link layer test mode where repeated lane alignment sequence (as specified in JESD204B Section 5.3.3.8.2) sent on all lanes.	0x1	R/W
		[1]	FACI	0 1	Frame alignment character insertion enabled (JESD204B Section 5.3.3.4). Frame alignment character insertion disabled. For debug only (JESD204B Section 5.3.3.4).	0x0	R/W
		[0]	Link control	0 1	JESD204B serial transmit link enabled. Transmission of the /K28.5/ characters for code group synchronization is controlled by the SYNC~ signal. JESD204B serial transmit link powered down (held in reset and clock gated).	0x0	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x021	JESD204B Link Control 2	[7:6]	SYNCINB± pin control	0 10 11	Normal mode. Ignore SYNCINB± (force CGS). Ignore SYNCINB± (force ILAS/user data).	0x0	R/W
		[5]	SYNCINB± pin invert	0 1	SYNCINB± pin not inverted. SYNCINB± pin inverted.	0x0	R/W
		[4]	Long transport layer test	0 1	JESD204B test samples disabled. JESD204B test samples enabled; long transport layer test sample sequence (as specified in JESD204B Section 5.1.6.3) sent on all link lanes.	0x0	R/W
		[3]	Short transport layer test	0 1	JESD204B test samples disabled. JESD204B test samples enabled; long transport layer test sample sequence (as specified in JESD204B Section 5.1.6.2) sent on all link lanes.	0x0	R/W
		[2]	8-bit/10-bit bypass	0 1	8-bit/10-bit enabled. 8-bit/10-bit bypassed (most significant 2 bits are 0).	0x0	R/W
		[1]	8-bit/10-bit bit invert	0 1	Normal. Invert a, b, c, d, e, f, g, h, I, and j symbols.	0x0	R/W
		[0]	link standby	0 1	Normal mode Link standby mode, clock is on, but only transimit K28.5 code.	0x0	R/W
0x022	JESD204B Link Control 3	[7:6]	Checksum mode	0 1 10 11	Checksum is the sum of all 8-bit registers in the link configuration table. Checksum is the sum of all individual link configuration fields (LSB aligned). Checksum is disabled (set to zero). For test purposes only. Unused.	0x1	R/W
		[5:4]	Test injection point	0 1 10	N' sample input. 10-bit data at 8-bit/10-bit output (for PHY testing). 8-bit data at scrambler input.	0x0	R/W
		[3:0]	JESD204B test mode patterns	0 1 10 11 100 101 110 111 1000 1110 1111	Normal operation (test mode disabled). Alternating checkerboard. 1/0 word toggle. 31-bit pseudorandom number (PN) sequence: x31 + x28 + 1. 23-bit PN sequence: x23 + x18 + 1. 15-bit PN sequence: x15 + x14 + 1. 9-bit PN sequence: x9 + x5 + 1. 7-bit PN sequence: x7 + x6 + 1. Ramp output. Continuous/repeat user test. Single user test.	0x0	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x023	JESD204B Link Control 4	[7:4]	ILAS delay	0	Transmit ILAS on first LMFC after SYNCINB± deasserted.	0x0	R/W
				1	Transmit ILAS on second LMFC after SYNCINB± deasserted.		
				10	Transmit ILAS on third LMFC after SYNCINB± deasserted.		
				11	Transmit ILAS on fourth LMFC after SYNCINB± deasserted.		
				100	Transmit ILAS on fifth LMFC after SYNCINB± deasserted.		
				101	Transmit ILAS on sixth LMFC after SYNCINB± deasserted.		
				110	Transmit ILAS on seventh LMFC after SYNCINB± deasserted.		
				111	Transmit ILAS on eighth LMFC after SYNCINB± deasserted.		
				1000	Transmit ILAS on ninth LMFC after SYNCINB± deasserted.		
				1001	Transmit ILAS on tenth LMFC after SYNCINB± deasserted.		
				1010	Transmit ILAS on eleventh LMFC after SYNCINB± deasserted.		
				1011	Transmit ILAS on twelfth LMFC after SYNCINB± deasserted.		
				1100	Transmit ILAS on thirteenth LMFC after SYNCINB± deasserted.		
				1101	Transmit ILAS on fourteenth LMFC after SYNCINB± deasserted.		
				1110	Transmit ILAS on fifteenth LMFC after SYNCINB± deasserted.		
				1111	Transmit ILAS on sixteenth LMFC after SYNCINB± deasserted.		
		[3]	Reserved		Reserved.	0x0	R
		[2:0]	Link layer test mode	0	Normal operation (link layer test mode disabled).	0x0	R/W
				1	Continuous sequence of /D21.5/ characters.		
				10	Reserved.		
				11	Reserved.		
				100	Modified RPAT test sequence.		
				101	JSPAT test sequence.		
				110	JTSPAT test sequence.		
				111	Reserved.		
0x024	JESD204B LMFC offset	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	LMFC phase offset value		Local multiframe clock (LMFC) phase offset value (in frame clocks). Refer to the Deterministic Latency section.	0x0	R/W
0x025	JESD204B scrambling and number lanes (L) configuration	[7]	JESD204B scrambling (SCR)	0	JESD204B scrambler disabled (SCR = 0).	0x1	R/W
				1	JESD204B scrambler enabled (SCR = 1).		
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	JESD204B lanes (L)	0	One lane per link (L = 1).	0xB	R/W
				1	Two lanes per link (L = 2).		
				11	Four lanes per link (L = 4).		
				…			
				1111	Eight lanes per Link (L = 16).		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x026	JESD204B link number of octets per frames (F)	[7:0]	JESD204B F configuration		JESD204B number of octets per frame (F = JESD204B F configuration + 1)	0x1	R/W
				0	F = 1.		
				1	F = 2.		
				10	F = 3.		
				11	F = 4.		
				101	F = 6.		
				111	F = 8.		
				1111	F = 16.		
0x027	JESD204B link number of frames per multiframe (K)	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JESD204B K configuration		JESD204B number of frames per multiframe (K = JESD204B K configuration + 1). Only values where F × K is divisible by 4 can be used.	0x1F	R/W
0x028	JESD204B link number of converters (M)	[7:0]	JESD204B M configuration		JESD204B number of converters per link/device (M = JESD204B M configuration).	0x0	R/W
				0	Link connected to one virtual converter (M = 1).		
				1	Link connected to two virtual converters (M = 2).		
				11	Link connected to four virtual converters (M = 4).		
				111	Link connected to eight virtual converters (M = 8).		
0x029	JESD204B number of control bits (CS) and ADC resolution (N)	[7:6]	Number of control bits (CS) per sample	0	No control bits (CS = 0).	0x0	R/W
				1	1 control bit (CS = 1), Control Bit 2 only.		
				10	2 control bits (CS = 2), Control Bit 2 and Control Bit 1 only.		
				11	3 control bits (CS = 3), all control bits (Control Bit 2, Control Bit 1, and Control Bit 0).		
		[5]	Reserved		Reserved.	0x0	R
		[4:0]	ADC converter resolution (N)	110	N = 7-bit resolution.	0xB	R/W
				111	N = 8-bit resolution.		
				1000	N = 9-bit resolution.		
				1001	N = 10-bit resolution.		
				1010	N = 11-bit resolution.		
				1011	N = 12-bit resolution.		
				1100	N = 13-bit resolution.		
				1101	N = 14-bit resolution.		
				1110	N = 15-bit resolution.		
				1111	N = 16-bit resolution.		
0x02A	JESD204B SCV NP configuration	[7:5]	Subclass support	0	Subclass 0.	0x0	R/W
				1	Subclass 1.		
		[4:0]	ADC number of bits per sample(N')	111	N' = 8.	0xB	R/W
				1011	N' = 12.		
				1111	N' = 16.		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x02B	JESD204B JV S configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Samples per converter frame cycle (S)		Samples per converter frame cycle (S = Register 0x0591, Bits[4:0] + 1).	0xF	R
0x02C	JESD204B HD CF configuration	[7]	HD value	0 1	High density format disabled. High density format enabled.	0x1	R
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	Control words per frame clock cycle per link (CF)		Number of control words per frame clock cycle per link. (CF = 0)	0x0	R
0x02D	JESD204B DID configuration	[7:0]	JESD204B Tx DID value		JESD204B serial device identification (DID) number.	0x0	R/W
0x02E	JESD204B BID configuration	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	JESD204B Tx BID value		JESD204B serial bank identification (BID) number (extension to DID).	0x0	R/W
0x030	JESD204B LID0 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 0 LID value		JESD204B serial lane identification (LID) number for Lane 0.	0x0	R/W
0x031	JESD204B LID1 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 1 LID value		JESD204B serial lane identification (LID) number for Lane 1.	0x1	R/W
0x032	JESD204B LID2 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 2 LID value		JESD204B serial lane identification (LID) number for Lane 2.	0x2	R/W
0x033	JESD204B LID3 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 3 LID value		JESD204B serial lane identification (LID) number for Lane 3.	0x3	R/W
0x034	JESD204B LID4 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 4 LID value		JESD204B serial lane identification (LID) number for Lane 4.	0x4	R/W
0x035	JESD204B LID5 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 5 LID value		JESD204B serial lane identification (LID) number for Lane 5.	0x5	R/W
0x036	JESD204B LID6 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 6 LID value		JESD204B serial lane identification (LID) number for Lane 6.	0x6	R/W
0x037	JESD204B LID7 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 7 LID value		JESD204B serial lane identification (LID) number for Lane 7.	0x7	R/W
0x038	JESD204B LID8 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 8 LID value		JESD204B serial lane identification (LID) number for Lane 8.	0x8	R/W
0x039	JESD204B LID9 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 9 LID value		JESD204B serial lane identification (LID) number for Lane 9.	0x9	R/W

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x03A	JESD204B LID10 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 10 LID value		JESD204B serial lane identification (LID) number for Lane 10.	0xA	R/W
0x03B	JESD204B LID11 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 11 LID value		JESD204B serial lane identification (LID) number for Lane 11.	0xB	R/W
0x03C	JESD204B LID12 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 12 LID value		JESD204B serial lane identification (LID) number for Lane 12.	0xC	R/W
0x03D	JESD204B LID13 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 13 LID value		JESD204B serial lane identification (LID) number for Lane 13.	0xD	R/W
0x03E	JESD204B LID14 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 14 LID value		JESD204B serial lane identification (LID) number for Lane 14.	0xE	R/W
0x03F	JESD204B LID15 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 15 LID value		JESD204B serial lane identification (LID) number for Lane 15.	0xF	R/W
0x040	JESD204B Lane Assign 1	[7:4]	SERDOUT1± lane assignment		Physical Lane 1 assignment.	0x1	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1 (default).		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				x	Logical Lane x.		
				1111	Logical Lane 15.		
		[3:0]	SERDOUT0± lane assignment		Physical Lane 0 assignment.	0x0	R/W
				0	Logical Lane 0 (default).		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				x	Logical Lane x.		
				1111	Logical Lane 15.		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x041	JESD204B Lane Assign 2	[7:4]	SERDOUT3± lane assignment		Physical Lane 3 assignment.	0x3	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3 (default).		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				x	Logical Lane x.		
				1111	Logical Lane 15.		
		[3:0]	SERDOUT2± lane assignment		Physical Lane 2 assignment.	0x2	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1		
				10	Logical Lane 2 (default).		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				x	Logical Lane x.		
				1111	Logical Lane 15.		
0x042	JESD204B Lane Assign 3	[7:4]	SERDOUT5± lane assignment		Physical Lane 5 assignment.	0x5	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5 (default).		
				x	Logical Lane x.		
				1111	Logical Lane 15.		
		[3:0]	SERDOUT4± lane assignment		Physical Lane 4 assignment.	0x4	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4 (default).		
				101	Logical Lane 5.		
				x	Logical Lane x.		
				1111	Logical Lane 15.		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x043	JESD204B Lane Assign 4	[7:4]	SERDOUT7± lane assignment		Physical Lane 7 assignment.	0x7	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				111	Logical Lane 7 (default).		
				1111	Logical Lane 15.		
		[3:0]	SERDOUT6± lane assignment		Physical Lane 6 assignment.	0x6	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				110	Logical Lane 6 (default).		
				1111	Logical Lane 15.		
0x044	JESD204B Lane Assign 5	[7:4]	SERDOUT9± lane assignment		Physical Lane 9 assignment.	0x9	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1001	Logical Lane 9 (default).		
				1111	Logical Lane 15.		
		[3:0]	SERDOUT8± lane assignment		Physical Lane 8 assignment.	0x8	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1000	Logical Lane 8 (default).		
				1111	Logical Lane 15.		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x045	JESD204B Lane Assign 6	[7:4]	SERDOUT11± lane assignment		Physical Lane 11 assignment.	0xB	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1011	Logical Lane 11 (default).		
				1111	Logical Lane 15.		
		[3:0]	SERDOUT10± lane assignment		Physical Lane 10 assignment.	0xA	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1010	Logical Lane 10 (default).		
				1111	Logical Lane 15.		
0x046	JESD204B Lane Assign 7	[7:4]	SERDOUT13± lane assignment		Physical Lane 13 assignment.	0xD	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1101	Logical Lane 13 (default).		
				1111	Logical Lane 15.		
		[3:0]	SERDOUT12± lane assignment		Physical Lane 12 assignment.	0xC	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1100	Logical Lane 12 (default).		
				1111	Logical Lane 15.		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x047	JESD204B Lane Assign 7	[7:4]	SERDOUT15± lane assignment		Physical Lane 15 assignment.	0xF	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15 (default).		
		[3:0]	SERDOUT14± lane assignment		Physical Lane 14 assignment.	0xE	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1110	Logical Lane 14 (default).		
				1111	Logical Lane 15.		
0x048	SERDOUTx± data invert	[7]	Invert SERDOUT7± data		Invert SERDOUT7± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[6]	Invert SERDOUT6± data		Invert SERDOUT6± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[5]	Invert SERDOUT5± data		Invert SERDOUT5± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[4]	Invert SERDOUT4± data		Invert SERDOUT4± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[3]	Invert SERDOUT3± data		Invert SERDOUT3± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[2]	Invert SERDOUT2± data		Invert SERDOUT2± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[1]	Invert SERDOUT1± data		Invert SERDOUT1± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[0]	Invert SERDOUT0± data		Invert SERDOUT0± data.	0x0	R/W
				0	Normal.		
				1	Invert.		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x049	SERDOUTx± data invert	[7]	Invert SERDOUT15± data		Invert SERDOUT15± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[6]	Invert SERDOUT14± data		Invert SERDOUT14± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[5]	Invert SERDOUT13± data		Invert SERDOUT13± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[4]	Invert SERDOUT12± data		Invert SERDOUT12± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[3]	Invert SERDOUT11± data		Invert SERDOUT11± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[2]	Invert SERDOUT10± data		Invert SERDOUT10± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[1]	Invert SERDOUT9± data		Invert SERDOUT9± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[0]	Invert SERDOUT8± data		Invert SERDOUT8± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
0x050	JESD204B Checksum 0 configuration	[7:0]	lane0_chksum		Serial checksum value for Lane 0. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 0) mod 256.		R
0x051	JESD204B Checksum 1 configuration	[7:0]	lane1_chksum		Serial checksum value for Lane 1. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 1) mod 256.		R
0x052	JESD204B Checksum 2 configuration	[7:0]	lane2_chksum		Serial checksum value for Lane 2. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 2) mod 256.		R
0x053	JESD204B Checksum 3 configuration	[7:0]	lane3_chksum		Serial checksum value for Lane 3. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 3) mod 256.		R
0x054	JESD204B Checksum 4 configuration	[7:0]	lane4_chksum		Serial checksum value for Lane 4. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 4) mod 256.		R
0x055	JESD204B Checksum 5 configuration	[7:0]	lane5_chksum		Serial checksum value for Lane 5. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 5) mod 256.		R
0x056	JESD204B Checksum 6 configuration	[7:0]	lane6_chksum		Serial checksum value for Lane 6. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 6) mod 256.		R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x057	JESD204B Checksum 7 configuration	[7:0]	lane7_chksum		Serial checksum value for Lane 7. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 7) mod 256.		R
0x058	JESD204B Checksum 8 configuration	[7:0]	lane8_chksum		Serial checksum value for Lane 8. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 8) mod 256.		R
0x059	JESD204B Checksum 9 configuration	[7:0]	lane9_chksum		Serial checksum value for Lane 9. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 9) mod 256.		R
0x05A	JESD204B Checksum 10 configuration	[7:0]	lane10_chksum		Serial checksum value for Lane 10. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 10) mod 256.		R
0x05B	JESD204B Checksum 11 configuration	[7:0]	lane11_chksum		Serial checksum value for Lane 11. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 11) mod 256.		R
0x05C	JESD204B Checksum 12 configuration	[7:0]	lane12_chksum		Serial checksum value for Lane 12. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 12) mod 256.		R
0x05D	JESD204B Checksum 13 configuration	[7:0]	lane13_chksum		Serial checksum value for Lane 13. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 13) mod 256.		R
0x05E	JESD204B Checksum 14 configuration	[7:0]	lane14_chksum		Serial checksum value for Lane 14. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 14) mod 256.		R
0x05F	JESD204B Checksum 15 configuration	[7:0]	lane15_chksum		Serial checksum value for Lane 15. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 15) mod 256.		R
0x60	PMA fifo wr enable	[7:0]	dbg_fifo_wr[7:0]		fifo wr enable for lane 0~7		R
0x61	PMA fifo wr enable	[7:0]	dbg_fifo_wr[15:8]		fifo wr enable for lane 8~15		R
0x62	PMA fifo rd enable	[7:0]	dbg_fifo_rd[7:0]		fifo rd enable for lane 0~7		R
0x63	PMA fifo rd enable	[7:0]	dbg_fifo_rd[15:8]		fifo rd enable for lane 8~15		R
0x64	PMA fifo empty	[7:0]	dbg_fifo_empty[7:0]		fifo empty for lane 0~7		R
0x65	PMA fifo empty	[7:0]	dbg_fifo_empty[15:8]		fifo empty for lane 8~15		R
0x66	PMA fifo full	[7:0]	dbg_fifo_full[7:0]		fifo full for lane 0~7		R
0x67	PMA fifo full	[7:0]	dbg_fifo_full[15:8]		fifo full for lane 8~15		R
0x68	PMA ready	[7:0]	dbg_pma_ready[7:0]		pma ready for lane 0~7		R
0x69	PMA ready	[7:0]	dbg_pma_ready[15:8]		pm ready for lane 8~15		R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x6A	PMA fifo rd start	[7:0]	dbg_rd_start[7:0]		fifo rd start for lane 0~7		R
0x6B	PMA fifo rd start	[7:0]	dbg_rd_start[15:8]		fifo rd start for lane 8~15		R
0x6C	PMA fifo wr start	[7:6]	Reserved		Reserved.		R
		[0]	dbg_wr_start		fifo write start for all lanes		R

PMA PHY Register

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x00	pll_cfg0	[7:0]	JESD204B pll cfg0			8'b0111,0101	R/W
		[7:5]	pll_cp_itrim	011	cp current trimming bits 3'b000: 50u 3'b001:100u 3'b010:150u 3'b011:200u default 3'b100:250u 3'b101:300u 3'b110:350u 3'b111:400u		R/W
		[4:3]	pll_cp_rsv	10	cp reset voltage trimming bits 2'b00: (1-12.5%)*vrst voltage 2'b01: (1-6.25%)*vrst voltage 2'b10: vrst voltage default 2'b11: (1+6.25%)*vrst voltage		R/W
		[2:1]	pll_cp_ls	10	cp level shift voltage trimming bits 2'b00: (1+12.5%)*vls voltage 2'b01: vls voltage 2'b10: vls voltage 2'b11: (1+12.5%)*vls voltage		R/W
		[0]	pll_lock_en	1	pll lock detect enable 1'b0: disable 1'b1: enable		R/W
0x01	pll_cfg1	[7:0]	JESD204B pll cfg1			8'b1010,1010	R/W
		[7:5]	pll_lpf_rtrim	101	lpf resistor trimming bits 3'b000: 10k 3'b001: 9k 3'b010: 8k 3'b011: 7k 3'b100: 6k 3'b101: 5k default 3'b110: 4k 3'b111: 3k		R/W
		[4:3]	pll_div2_itrim	01	high speed div2 current trimming bits 2'b00: 1.6mA 2'b01: 2mA 2'b10: 2.4mA 2'b11: 2.8mA		R/W
		[2:1]	pll_div2_buf	01	high speed div2buf current trimming bits 2'b00: 2mA 2'b01: 3mA 2'b10: 3mA 2'b11: 4mA		R/W
		[0]	RSV	0	Reserved		R/W
0x02	pll_cfg2	[7:0]	JESD204B pll cfg2			8'b0100,0010	R/W
		[7]	pll_vco_rtrim_mannul	0	pll vco rtrim mannul trimming bit 1'b0: auto mode 1'b1: mannul mode		
		[6:2]	pll_vco_rtrim_reg	10000	pll vco rtrim code in mannul mode		
		[1:0]	pll_fbdiv<1:0>	10	pll feedback divider ratio trimming bits 2'b00: /16 2'b01: /32 2'b10: /20 default 2'b11: /40		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x03	pll_cfg3	[7:0]	JESD204B pll cfg3			8'b0001,0100	R/W
		[7]	pll_tsten	0	pll test enable 1'b0: disable 1'b1: enable		
		[6:5]	pll_atest_sel	00	pll analog voltage select 2'b00: no select 2'b01: select ldo voltage output 2'b10: select vcntl voltage output		
		[4:3]	pll_lock_factor	10	pll lock detect frequency compare mask select 2'b00:16'b1111 1111 1111 1000 2'b01:16'b1111 1111 1111 0000 2'b10:16'b1111 1111 1110 0000 default 2'b11:16'b1111 1111 1100 0000		
		[2:1]	pll_lock_coarse	10	pll lock detect frequency compare counter select 2'b00:16'd65535 2'b01:16'd4095 2'b10:16'd1023 default 2'b11:16'd255		
		[0]	RSV	0	Reserved		
0x04	pll_cfg4	[7:0]	JESD204B pll cfg4			8'b0100,0001	R/W
		[7]	pll_vco_crs_ovrden	0	vco code overwrite enable 1'0： disable 1'b1: enable		
		[6:1]	pll_vco_code	100000	vco overwrite code, mannul mode		
		[0]	pll_vco_ofst_en	1	ignore vco code offset enable 1'b0: disable, vco code with offset 1'b1: enable, ignore offset		
0x05	pll_cfg5	[7:0]	JESD204B pll cfg5			8'0001,1001	R/W
		[7]	pll_vco_band_sel	0	vco high band and low band select in mannul mode 1'b0：select high band 1'b1: select low band		
		[6:5]	pll_vco_accuracy	00	vco calibration perilod select 2b'00: 4095 default 2b'01: 1023 2b'10: 16383 2b'11: 65535		
		[4]	pll_vco_band_sel_auto	1	auto select vco high band and low band 1'b0：mannul mode 1'b1: auto mode		
		[3:2]	pll_vco_offset	10	offset of the vco coarse tuning code setting 2b'00: -1 2b'01: -2 2b'10: +1 2b'11: +2		
		[1:0]	pll_lock_latency_sel	01	waiting time trimming when pll in the closed loop pll 2b'00: 65535 2b'01: 16383 default 2b'10: 4095 2b'11: 1023		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x06	rcal_cfg0	[7:0]	JESD204B rcal cfg0			8'b0101,0110	R/W
		[7:6]	ircal50u_cal_ctl	01	current trimming for the resistor calibration block 2'b00:1mA*98% 2'b01:1mA 2'b10:1mA*1.02% 2'b11:1mA*1.04%		
		[5:4]	ircal50u_pll_ctl	01	pll calibration current trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[3:2]	ircal50u_tx_ctl	01	tx calibration current trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[1]	rcalenb_manual	1	resistor calibration mode 1'b0: manual mode 1'b1:auto mode		
		[0]	iref_testen	0	test enable for accurate 50u current for adc core 1'b0: disable 1'b1: enable		
0x07	rcal_cfg1	[7:0]	JESD204B rcal cfg1			8'b0000,0000	R/W
		[7:5]	txcal_offset	000	tx cailibration code offset 3'b000: rcal _tx[4:0]= rcal[4:0] 3'b001: rcal _tx[4:0]= rcal[4:0]+1 3'b010: rcal _tx[4:0]= rcal[4:0]+2 3'b011: rcal _tx[4:0]= rcal[4:0]+3 3'b100: rcal _tx[4:0]= rcal[4:0] 3'b101: rcal _tx[4:0]= rcal[4:0]-1 3'b110: rcal _tx[4:0]= rcal[4:0]-2 3'b111: rcal _tx[4:0]= rcal[4:0]-3		
		[4:2]	pllcal_offset	000	pll calibration code offset 3'b000: rcal _pll[4:0]= rcal[4:0] 3'b001: rcal _pll[4:0]= rcal[4:0]+1 3'b010: rcal _pll[4:0]= rcal[4:0]+2 3'b011: rcal _pll[4:0]= rcal[4:0]+3 3'b100: rcal _pll[4:0]= rcal[4:0] 3'b101: rcal _pll[4:0]= rcal[4:0]-1 3'b110: rcal _pll[4:0]= rcal[4:0]-2 3'b111: rcal _pll[4:0]= rcal[4:0]-3		
		[1:0]	RSV	00	Reserved		
0x08	tx_cfg0	[7:0]	JESD204B tx cfg0			8'b1110,0000	R/W
		[7:6]	tx_wide_mode, tx_divbyfive	11	tx data width select 2'b00: 16 bits 2'b01: 20 bits 2'b10: 32 bits 2'b11: 40 bits		
		[5:3]	tx_drvbiastrim	100	driver bias current trimming 3'b000: -40uA 3'b001: -30uA 3'b010: -20uA 3'b011: -10uA 3'b100: +0uA 3'b101: +10uA 3'b110: +20uA 3'b111: +30uA		
		[2:0]	tx_emppre	000	tx pre-cursor setting		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x09	tx_cfg1	[7:0]	JESD204B tx cfg1			8'b1000,0000	R/W
		[7:3]	tx_termprog	10000	tx code manual		
		[2]	tx_dcc_enb	0	tx duty cycle calibration enable, active low 1'b0: enable 1'b1: disable		
		[1]	tx_termcodesel	0	tx code mode select 1'b0: auto mode 1'b1: manual mode		
		[0]	tx_termtest	0	tx term test		
0x0A	tx_cfg2	[7:0]	JESD204B tx cfg2			8'b0000,0000	R/W
		[7]	tx_tstdiven	0	tx low speed data test enable 1'b0: disable 1'b1: enable		
		[6:3]	tx_amonsel	0000	tx analog test voltage select, detail see TestMux		
		[2]	tx_pdivsel<2>	0	tx post divider by 16 when it is enabled		
		[1]	tx_prbs_en	0	tx prbs enable 1'b0:disable 1'b1: enable		
		[0]	tx_prbs_mode	0	tx prbs mode select 1'b0: 0101 pattern 1'b1: prbs7 pattern		
0x0B	com_cfg0	[7:0]	JESD204B com cfg0			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6]	com_dig_tst_sel	0	digital signal select 1'b0: select refclk for com_tstclk<0> /select fbclk for com_tstclk<1> 1'b1: select tielow for com_tstclk<0> /select cfgclk for com_tstclk<1>		
		[5:0]	com_ana_tst_sel	000000	analog signal select detail see TestMux		
0x0C	bg_cfg0	[7:0]	JESD204B bg cfg0			8'b0101,0101	R/W
		[7:6]	ir50u_pll_ctrl	01	vbg/r current of pll trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[5:4]	ir50u_buff_ctrl	01	vbg/r current of buffer trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[3:2]	ir50u_rcal_ctrl	01	vbg/r current of rcal trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[1:0]	ir50u_spare_ctrl	01	vbg/r current of spare trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0D	bg_cfg1	[7:0]	JESD204B bg cfg1			8'b0110,0000	R/W
		[7:6]	bg_trimcom	01	vbg voltage trimming bits 2'b00:1.193v 2'b01:1.216v 2'b10:1.24v 2'b11:1.264v		
		[5:3]	bg_trimvco	100	vco voltage trimming bits 3'b000:1.119v 3'b001:1.144v 3'b010:1.168v 3'b011:1.193v 3'b100:1.216v 3'b101:1.24v 3'b110:1.264v 3'b111:1.288v		
		[2]	bg_safemode	0	bg safe mode enable 1'b0: normal mode 1'b1: safe mode		
		[1]	bg_testen	0	bg test enable 1'b0: disable 1'b1: enable		
		[0]	RSV	0	Reserved		
0x0E	pma_top_cfg0	[7:0]	JESD204B pma top cfg0			8'b1000,0000	R/W
		[7:6]	pma_top_buf_itrim	10	clock buffer trimming bits 2'b00: 2mA 2'b01: 3mA 2'b10: 3mA 2'b11: 4mA		
		[5]	RSV	0	Reserved		
		[4:0]	pma_top_clktst_sel	00000	pma top test signal select detail see TestMux		
0x0F	pma_top_cfg1	[7:0]	JESD204B pma top cfg1			8'b0000,0001	R/W
		[7]	bg_pwrdn	0	bg power down enable 1'b0: normal work 1'b1: power down	.	
		[6]	pll_pwrdn	0	pll power down enable 1'b0: normal work 1'b1: power down		
		[5:4]	RSV	000000	Reserved		
		[3]	pllck_dccfix	0	pllck duty cycle calibration fixed function 1'b0: normal work 1'b1: dcc output fixed to an equal level		
		[2]	pllck_dccenb	0	pllck duty cycle calibration enable, active low 1'b0: normal work 1'b1: disable pllck dcc funciton		
		[1:0]	pllck_dcctrim	01	dcc current trimming bits 2'b00: 0.6mA 2'b01: 0.9mA 2'b10: 1.2mA 2'b11: 1.5mA		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x10	adc_clk_stime	[7:0]	JESD204B adc clk wait time			8'b1000,0000	R/W
		[7:3]	cfg_clk_wait_time	10000	PMA reset sequence adc_clk stable time control bits: cycle = 2^adc_clk_stime 5'b00000: 1 cycles of Cfg_Clk; 5'b00001: 2^1 cycles of Cfg_Clk; 5'b00010: 2^2 cycles of Cfg_Clk; ….; 5'b10000: 2^16 cycles of Cfg_Clk; default ….; 5'b11111: 2^31 cycles of Cfg_Clk;		
		[2:0]	RSV	000	Reserved		
0x11	fsm_reset_seq	[7:0]	JESD204B fsm reset			8'b0000,0000	R/W
		[7]	top_seq_bypass	0	top sequence bypass 1'b0: normal work 1'b1: bypass		
		[6]	lnk_rdy	0	link_ready 1'b0: not ready 1'b1: link ready		
		[5]	rcal_enb	0	rcal enable,active low 1'b0: enable 1'b1: disable		
		[4]	pll_rstb	0	pll reset,active low 1'b0: reset 1'b1: normal work		
		[3]	tx_rstb	0	tx reset,active low 1'b0: reset 1'b1: normal work		
		[2]	rstb_d	0	mac reset,active low 1'b0: reset 1'b1: normal work		
		[1:0]	RSV	00	Reserved		
0x12	divider_cfg	[7:0]	JESD204B divider cfg in mannual			8'b0000,0000	R/W
		[7:6]	pll_mdiv	00	mdivider select config in mannual 2'b00: /1 2'b01: /2 2'b10: /4 2'b11: /8		
		[5:4]	tx_pdiv	00	pdivide select config in mannual 2'b00: /1 2'b01: /2 2'b10: /4 2'b11: /8		
		[3]	div_sel	0	1'b0: pll_mdiv/tx_pdiv use fsm value 1'b1: pll_mdiv/tx_pdiv use reg 0x12 bits [7:4].		
		[2]	adcdiv1	0	predivider in adc. 0: div 2 1: div 3		
		[1:0]	adcdiv0	00	predivider in adc. 00: div 1 01: div 2 10: div 4 11: div 8		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x13	time_1us_set	[7:0]	time count for 1us			8'b1000,1010	R/W
		[7:0]	time_1us	1000,1010	timer count for 1.25us at 110MHz		
0x14	tx_pwr_cfg0	[7:0]	tx power down config			8'b0000,0000	R/W
		[7:0]	tx_pwrdn	0000,0000	tx power down 1'b0: normal work 1'b1: power down bit<7>: control lane7 ... bit<0>: control lane0		
0x15	tx_pwr_cfg1	[7:0]	tx power down config			8'b0000,0000	R/W
		[7:0]	tx_pwrdn	0000,0000	tx power down 1'b0: normal work 1'b1: power down bit<7>: control lane15 ... bit<0>: control lane8		
0x16	pll_status	[7:0]	pll status			8'b0000,0000	R
		[7]	RSV	0	Reserved		
		[6]	pll_afc_fine_en		pll fine tuning mode indicator 1'b0: coarse tuning process 1'b1: fine tuning process		
		[5:0]	pll_vco_ctrim		vco band code		
0x17	rcal_code	[7:0]	rcal code			8'b0000,0000	R
		[7:5]	RSV	00	Reserved		
		[4:0]	rcal_code		resistor calibration code		
0x20	tx_drvamp_cfg0	[7:0]	tx drvamp cfg0			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane1	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane0	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x21	tx_drvamp_cfg1	[7:0]	tx drvamp cfg1			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane3	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane2	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
0x22	tx_drvamp_cfg2	[7:0]	tx drvamp cfg2			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane5	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane4	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x23	tx_drvamp_cfg3	[7:0]	tx drvamp cfg3			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane7	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane6	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
0x24	tx_drvamp_cfg4	[7:0]	tx drvamp cfg4			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane9	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane8	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x25	tx_drvamp_cfg5	[7:0]	tx drvamp cfg5			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane11	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane10	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
0x26	tx_drvamp_cfg6	[7:0]	tx drvamp cfg6			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane13	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane12	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x27	tx_drvamp_cfg7	[7:0]	tx drvamp cfg7			8'b0100,0100	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_drvamp_lane15	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_drvamp_lane14	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
0x28	tx_post_tap_cfg0	[7:0]	tx post tap cfg0			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane1	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane0	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x29	tx_post_tap_cfg1	[7:0]	tx post tap cfg1			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane3	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane2	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
0x2A	tx_post_tap_cfg2	[7:0]	tx post tap cfg2			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane5	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane4	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2B	tx_post_tap_cfg3	[7:0]	tx post tap cfg3			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane7	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane6	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
0x2C	tx_post_tap_cfg4	[7:0]	tx post tap cfg4			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane9	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane8	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2D	tx_post_tap_cfg5	[7:0]	tx post tap cfg5			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane11	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane10	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
0x2E	tx_post_tap_cfg6	[7:0]	tx post tap cfg6			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane13	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane12	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2F	tx_post_tap_cfg7	[7:0]	tx post tap cfg7			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6:4]	tx_post_tap_lane15	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[3]	RSV	0	Reserved		
		[2:0]	tx_post_tap_lane14	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		

9 封装尺寸 (Package Outline)

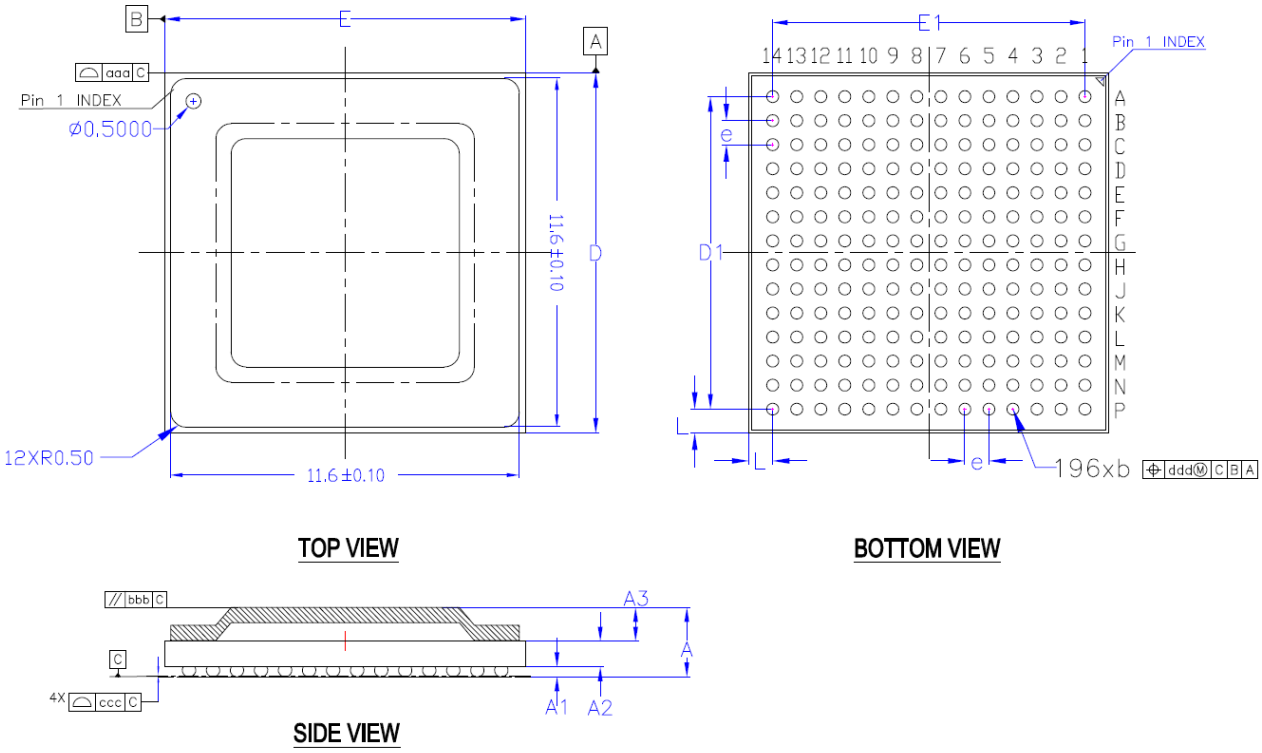


图 9-1. 封装尺寸

Dimensional Ref.

REF. Min.		Nom.	Max.
A	2.13	2.32	2.51
A1	0.30	0.35	0.40
A2	0.76	0.85	0.94
A3	1.07	1.12	1.17
D	11.9	12.0	12.1
E	11.9	12.0	12.1
D1	10.4 BSC		
E1	10.4 BSC		
L	0.8 REF		
e	0.8 BSC		
b	0.40	0.45	0.50
Tol. of Form & Position			
aaa	0.10		
bbb	0.10		
ccc	0.20		
ddd	0.05		

Notes:

1. All Dimensions are in Millimeters (Angles in Degrees).

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

10 订购指南 (Orderable Information)

型号	产品描述	温度范围	封装描述	封装选项
CAE2200	12 位 11.2Gsps 射频采样 ADC	-40℃ 至 +105℃	196 球- 倒装球栅阵列封装	FCBGA-196
CAE2400	12 位 5.6Gsps 射频采样 ADC	-40℃ 至 +105℃	196 球- 倒装球栅阵列封装	FCBGA-196

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